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(12) United States Patent
Zhu

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(54) **METHOD FOR SELECTIVELY MODIFYING SPACING BETWEEN PITCH MULTIPLIED STRUCTURES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Aug. 9, 2013**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 13/238,192, filed on Sep. 21, 2011, now Pat. No. 8,507,384, which is a continuation of application No. 12/053,513, filed on Mar. 21, 2008, now Pat. No. 8,030,218.

(51) **Int. Cl.**

H01L 21/311	(2006.01)
H01L 21/308	(2006.01)
H01L 21/033	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 21/3088*** (2013.01); ***H01L 21/31116*** (2013.01); ***H01L 21/0337*** (2013.01); ***H01L 21/0338*** (2013.01); ***H01L 21/76816*** (2013.01); *H01L 27/115* (2013.01); *H01L 27/118* (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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Primary Examiner — Shamim Ahmed
Assistant Examiner — Bradford Gates
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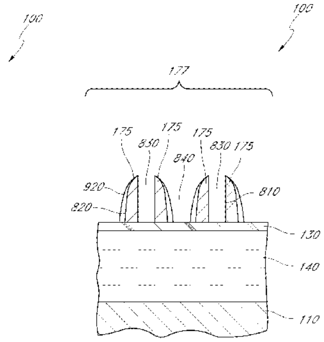
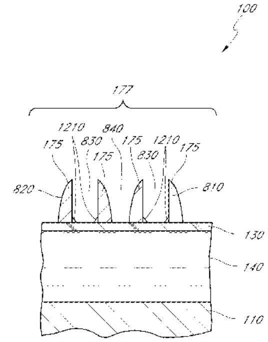
(57) **ABSTRACT**

Methods for circuit material processing are provided. In at least one such method, a substrate is provided with a plurality of overlying spacers. The spacers have substantially straight inner sidewalls and curved outer sidewalls. An augmentation material is formed on the plurality of spacers such that the inner or the outer sidewalls of the spacers are selectively expanded. The augmentation material can bridge the upper portions of pairs of neighboring inner sidewalls to limit deposition between the inner sidewalls. The augmentation material is selectively etched to form a pattern of augmented spacers having a desired augmentation of the inner or outer sidewalls. The pattern of augmented spacers can then be transferred to the substrate through a series of selective etches such that features formed in the substrate achieve a desired pitch.

20 Claims, 37 Drawing Sheets





(51) **Int. Cl.**

H01L 21/768	(2006.01)
H01L 27/115	(2006.01)
H01L 27/118	(2006.01)

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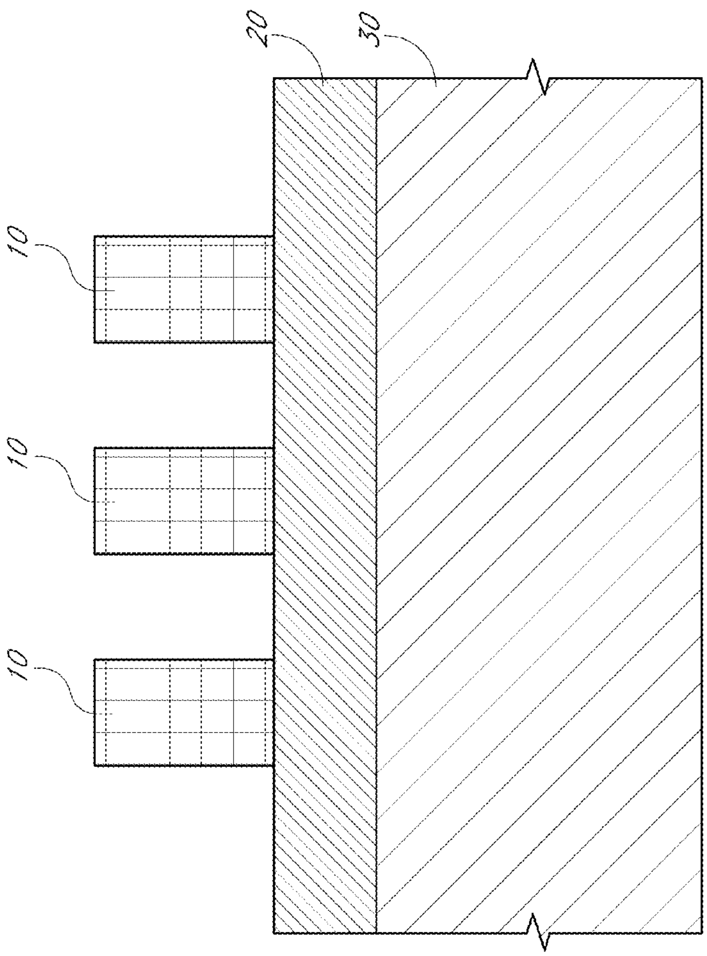

FIG. 1A
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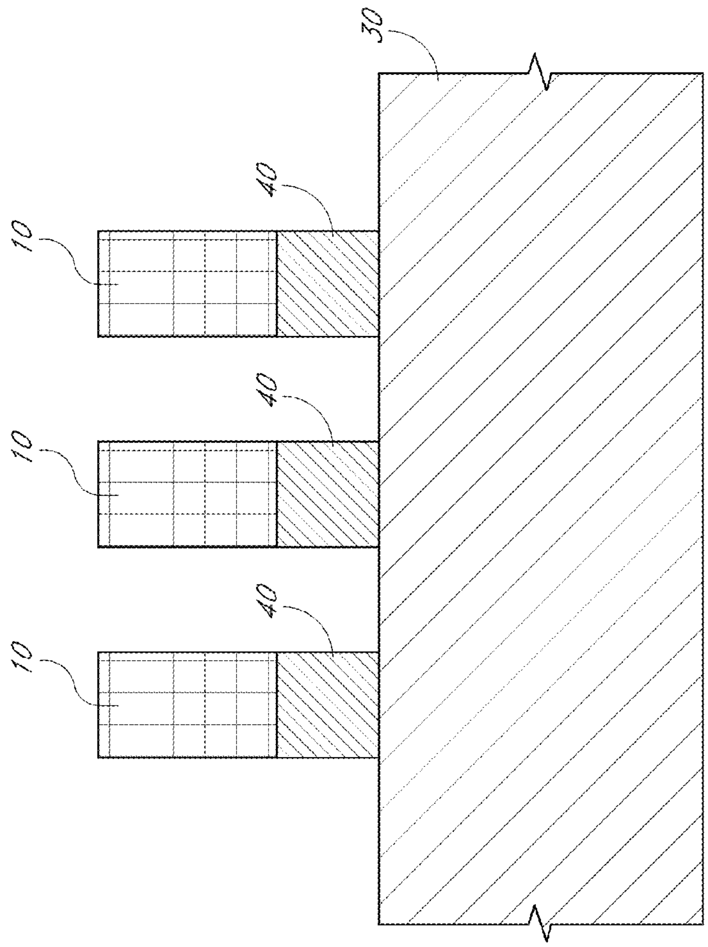


FIG. 1B
(PRIOR ART)

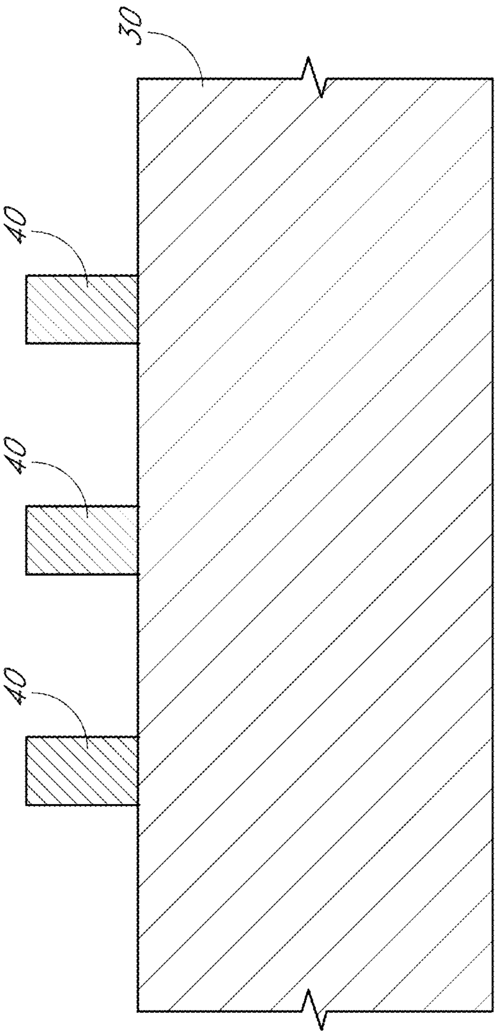


FIG. 1C
(PRIOR ART)

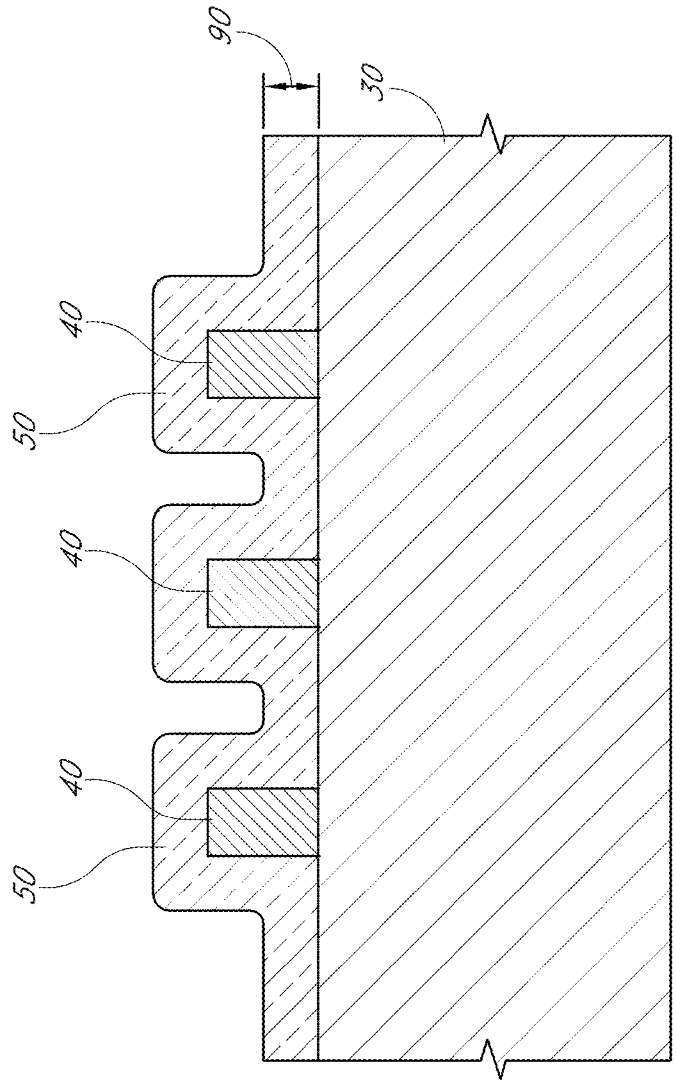


FIG. 1D
(PRIOR ART)

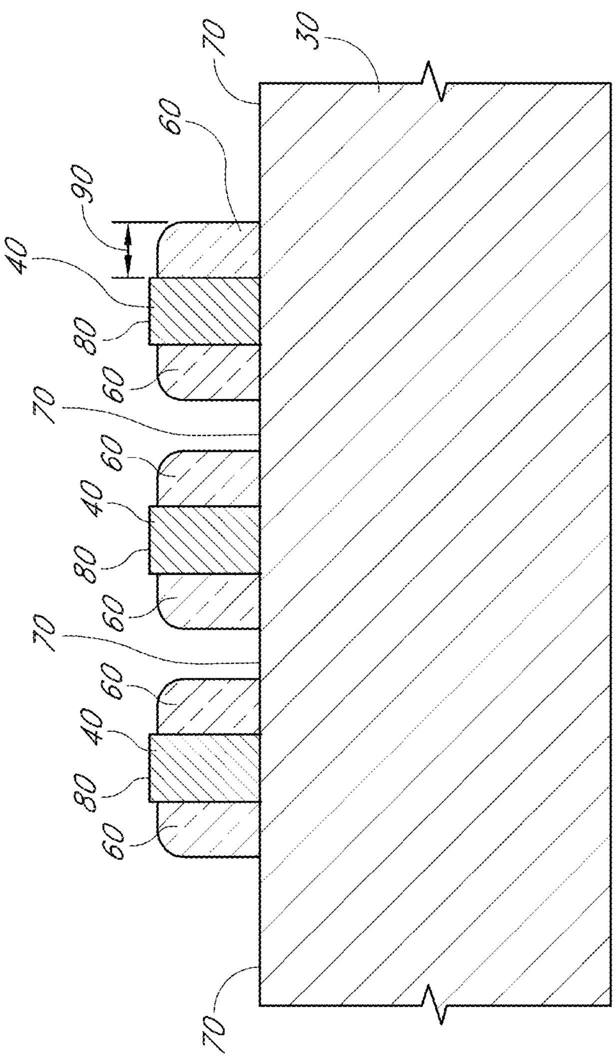


FIG. 1E
(PRIOR ART)

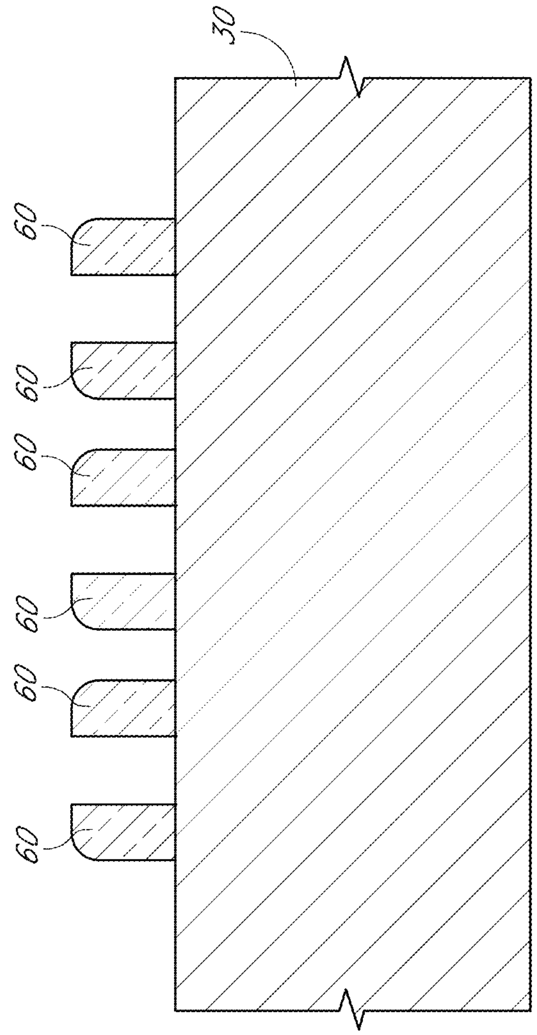


FIG. 1F
(PRIOR ART)

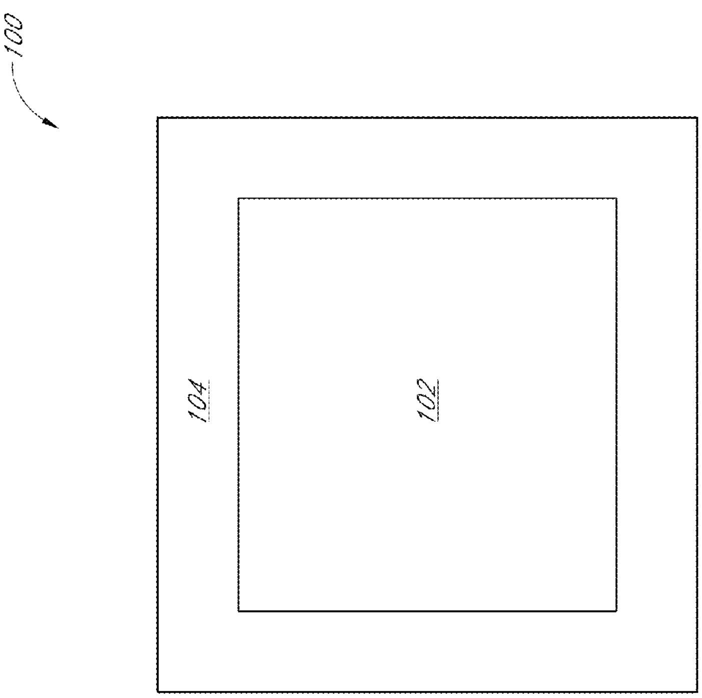


FIG. 2

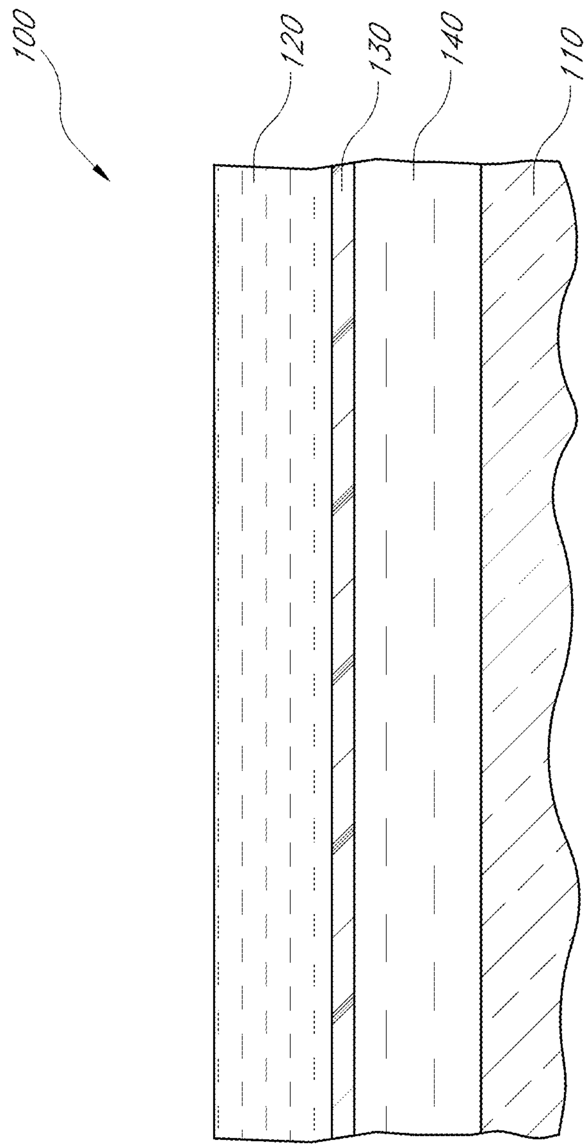
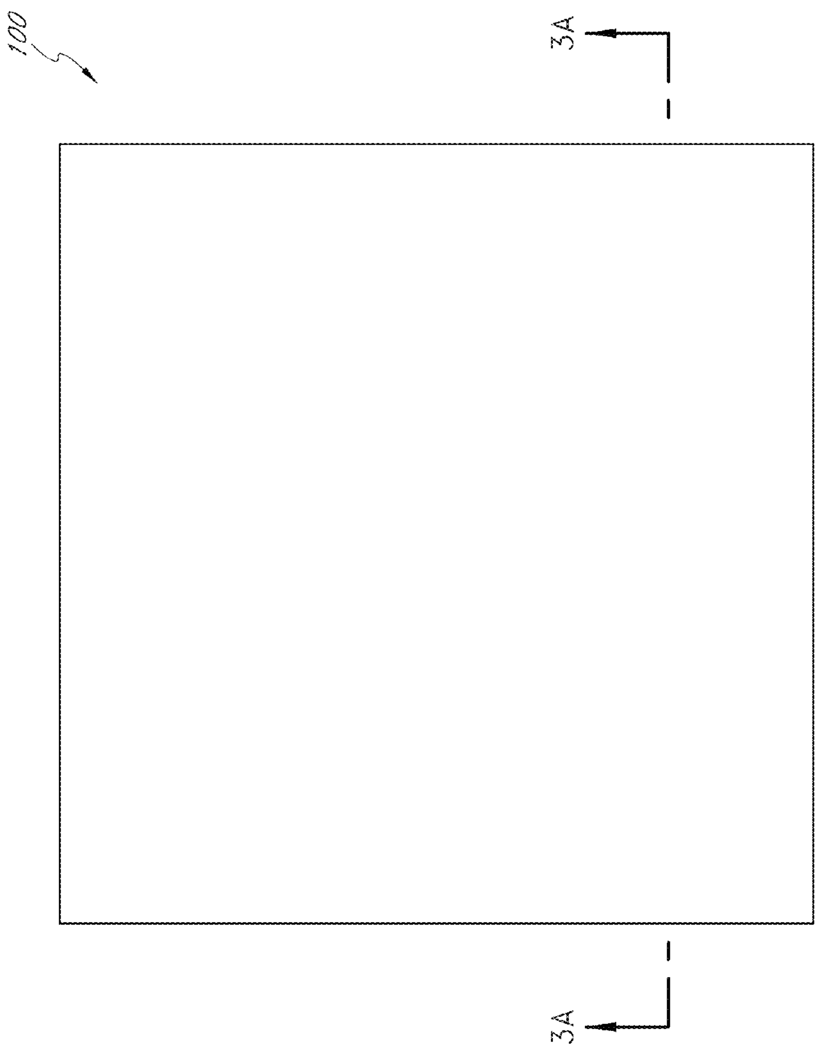


FIG. 3A



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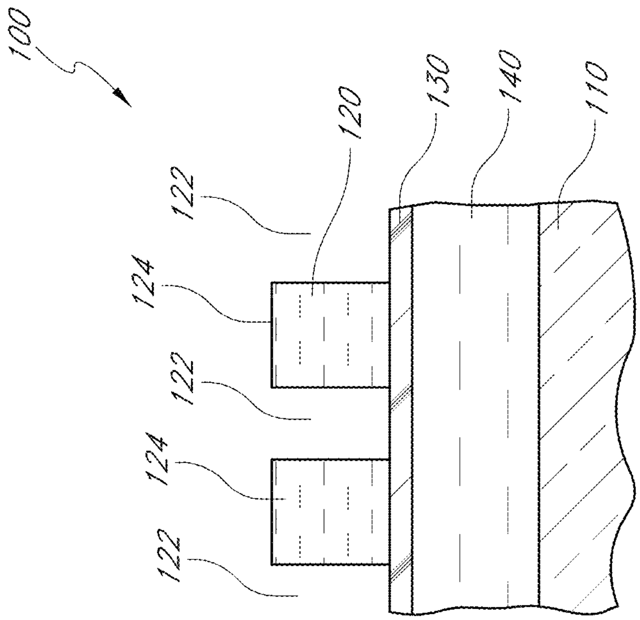


FIG. 4A

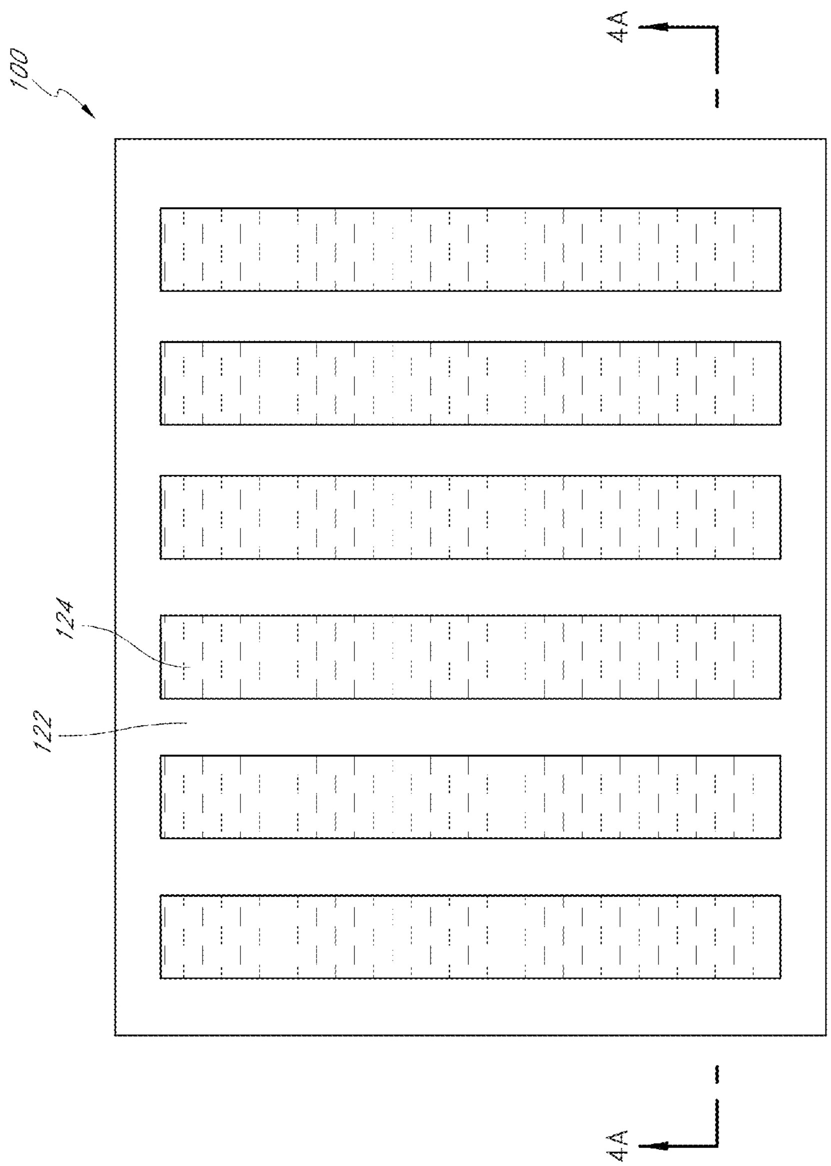


FIG. 4B

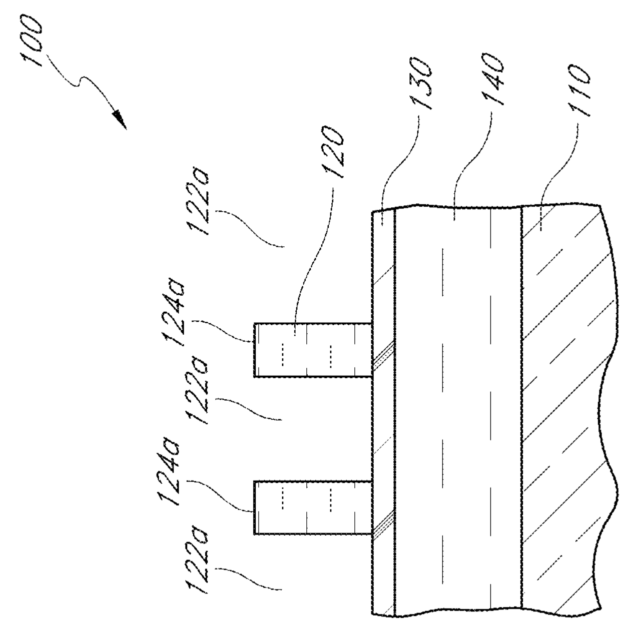


FIG. 5A

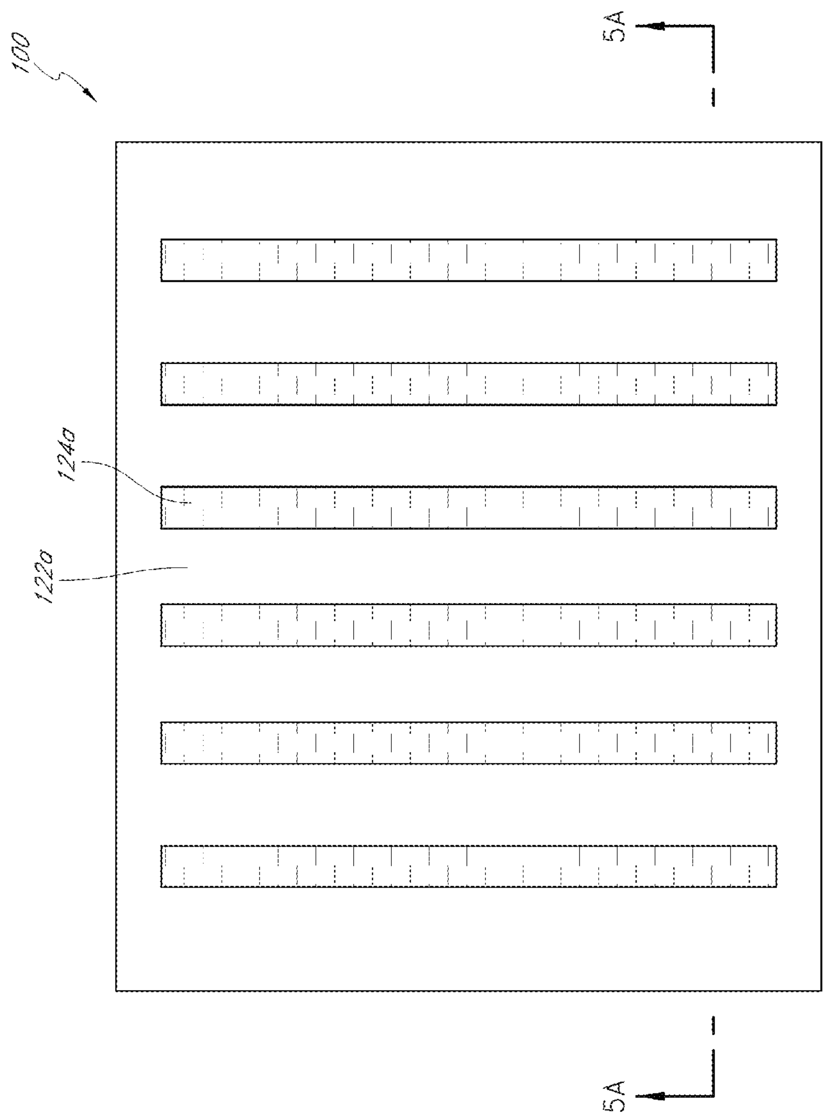


FIG. 5B

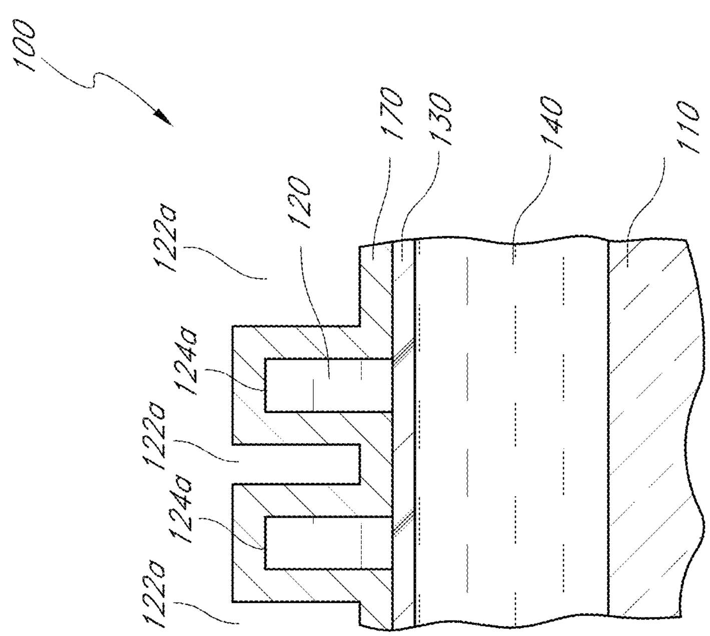


FIG. 6

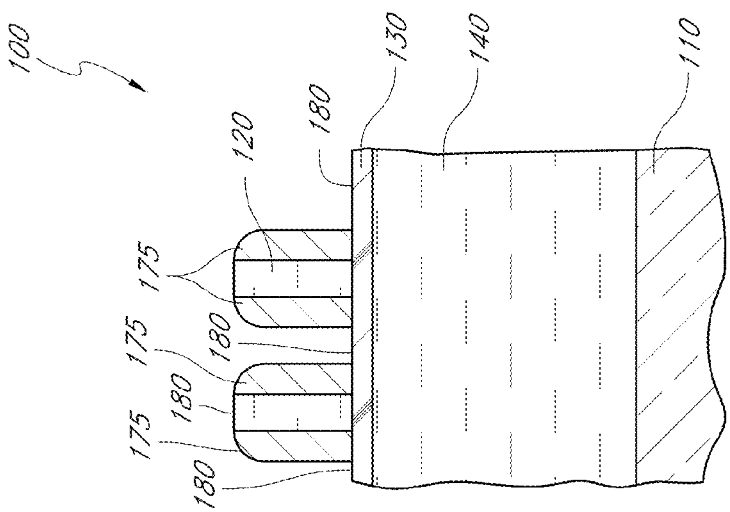


FIG. 7A

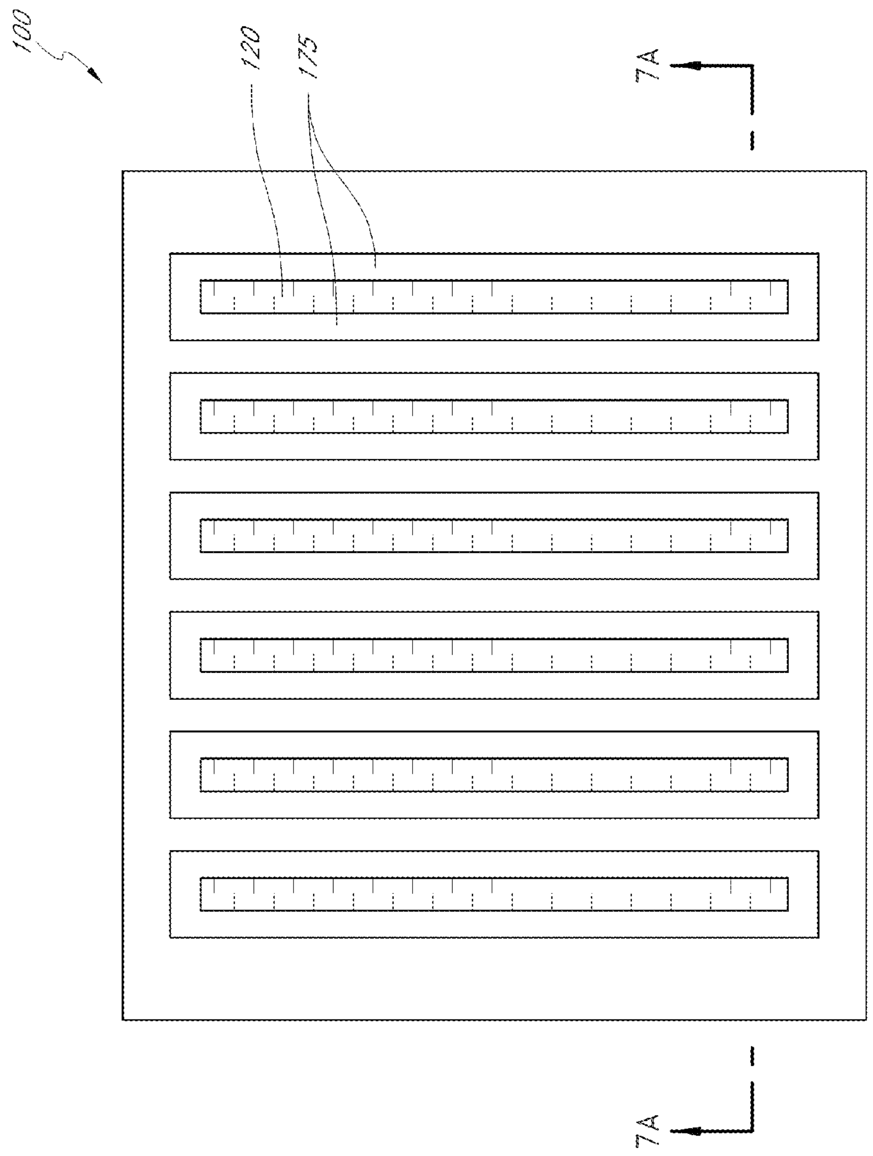


FIG. 7B

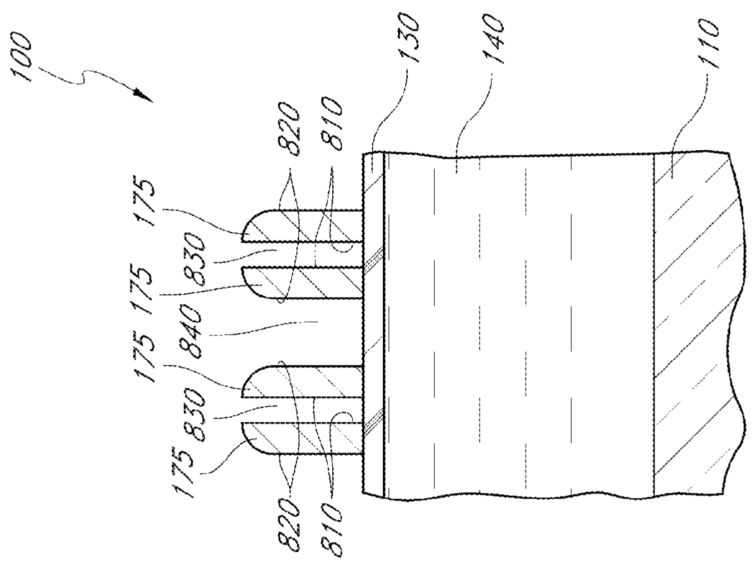


FIG. 8A

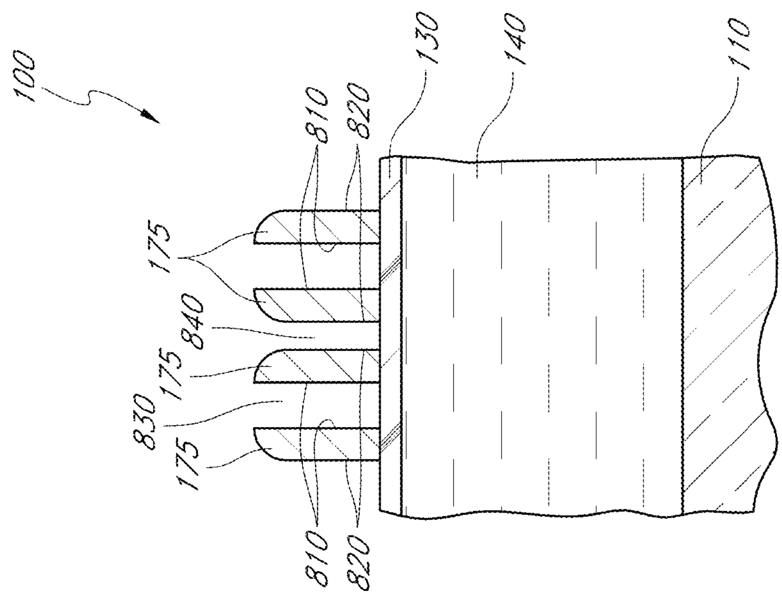


FIG. 8B

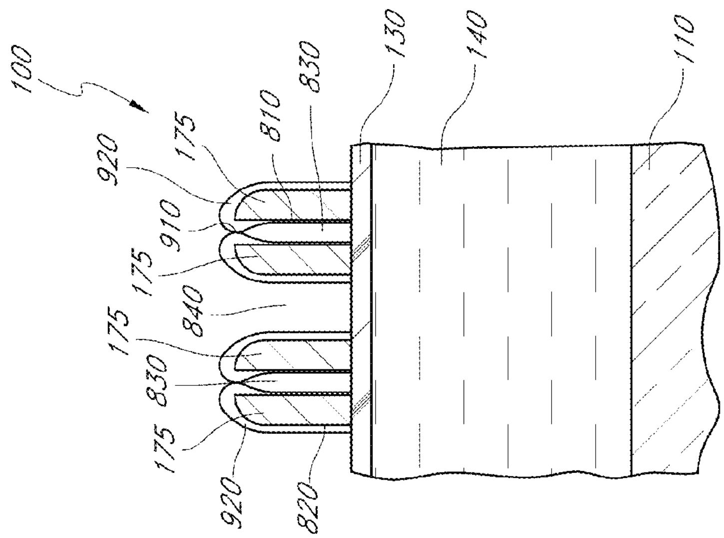


FIG. 9A

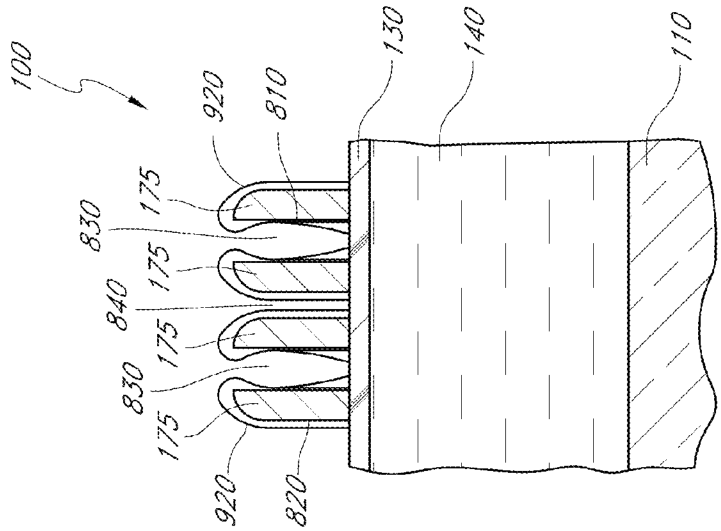


FIG. 9B

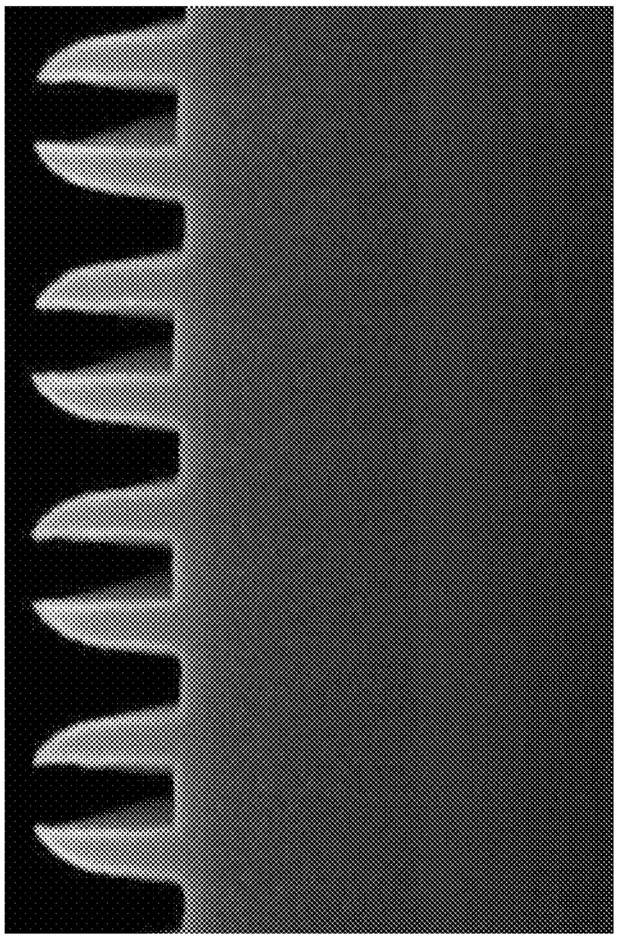


FIG. 10

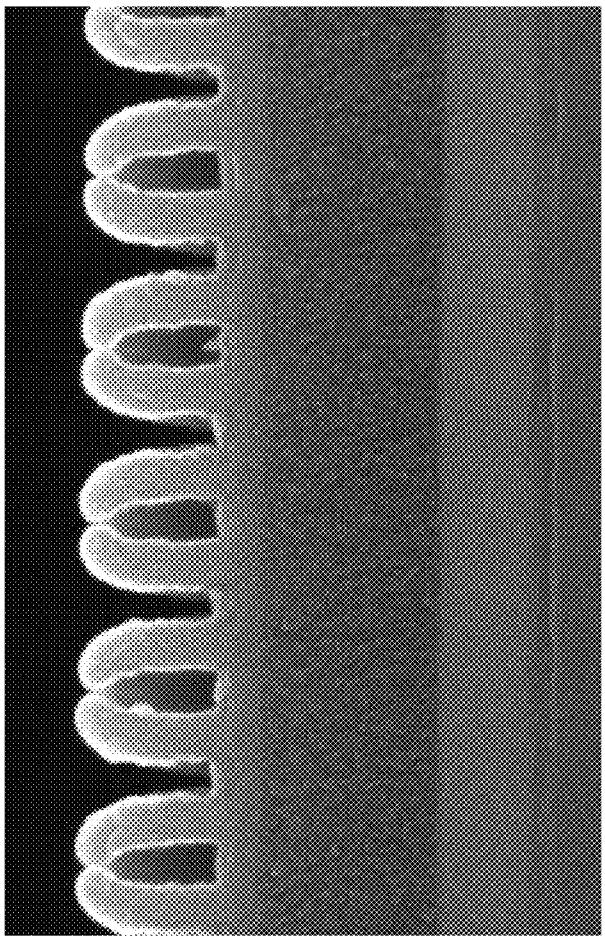


FIG. 11

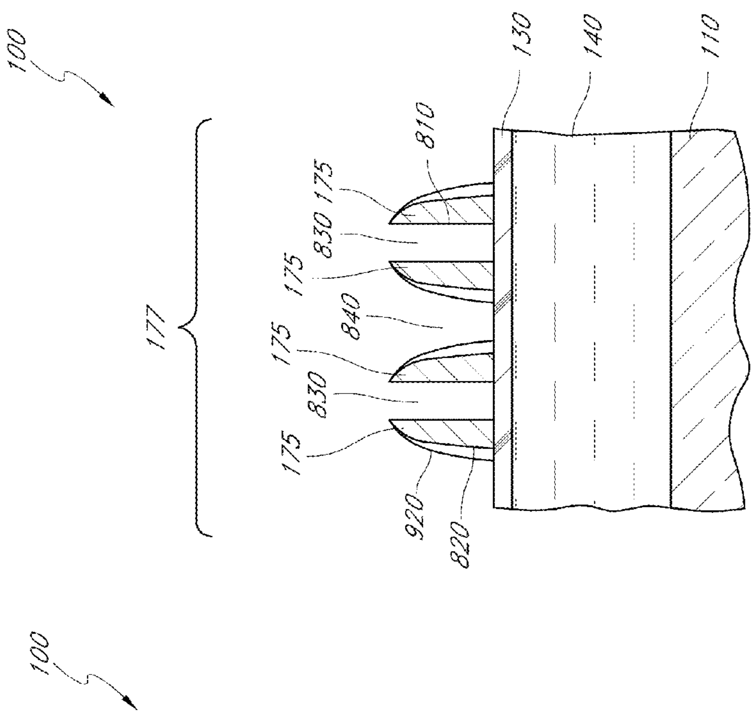
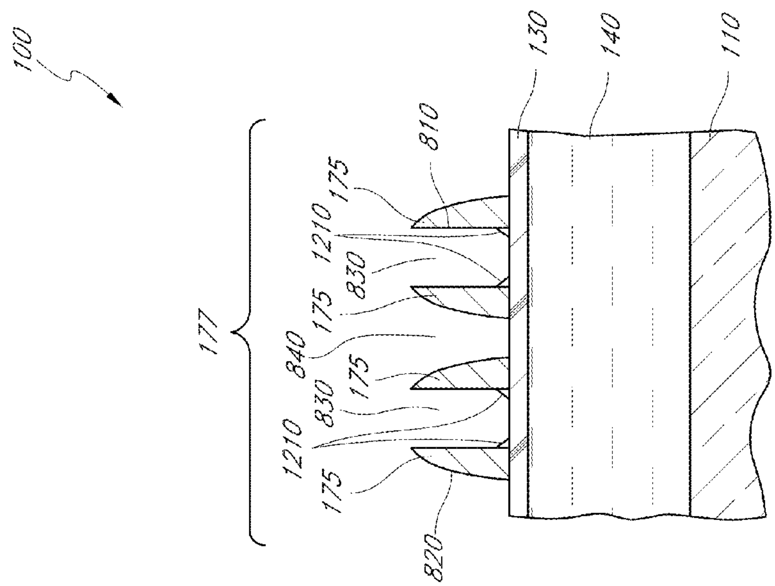

100
177
175
830
175
810
130
140
110
175
840
175
830
175
920
820
100

FIG. 12A



100
177
810
175
1210
830
175
840
175
830
1210
175
820
130
140
110

FIG. 12B

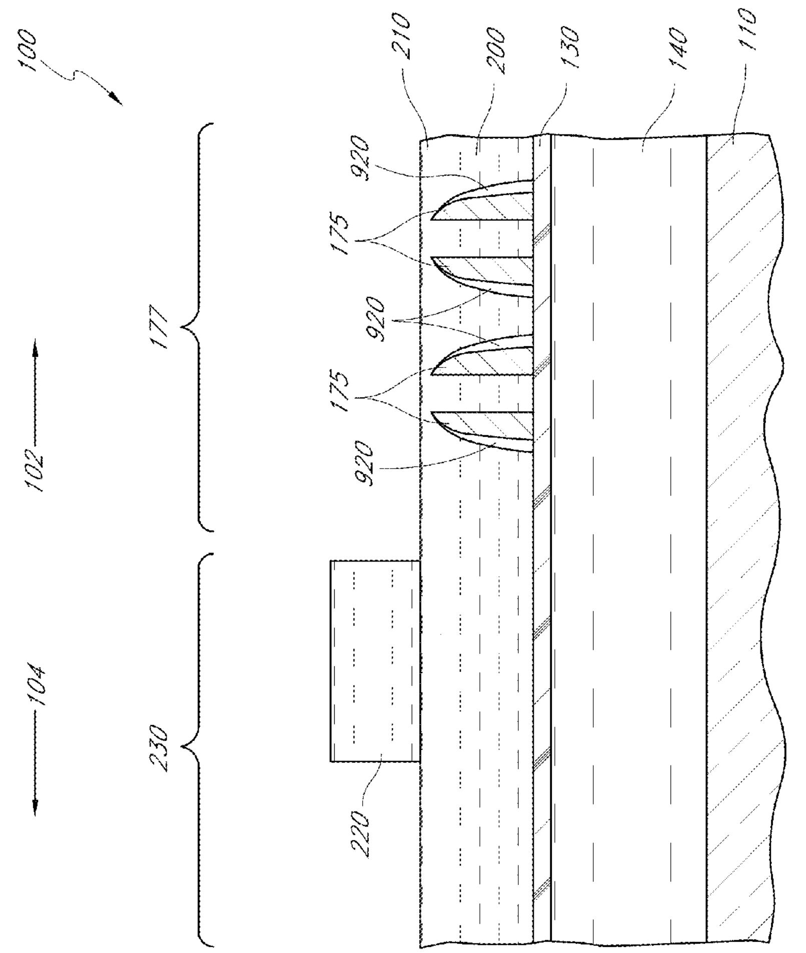


FIG. 13A

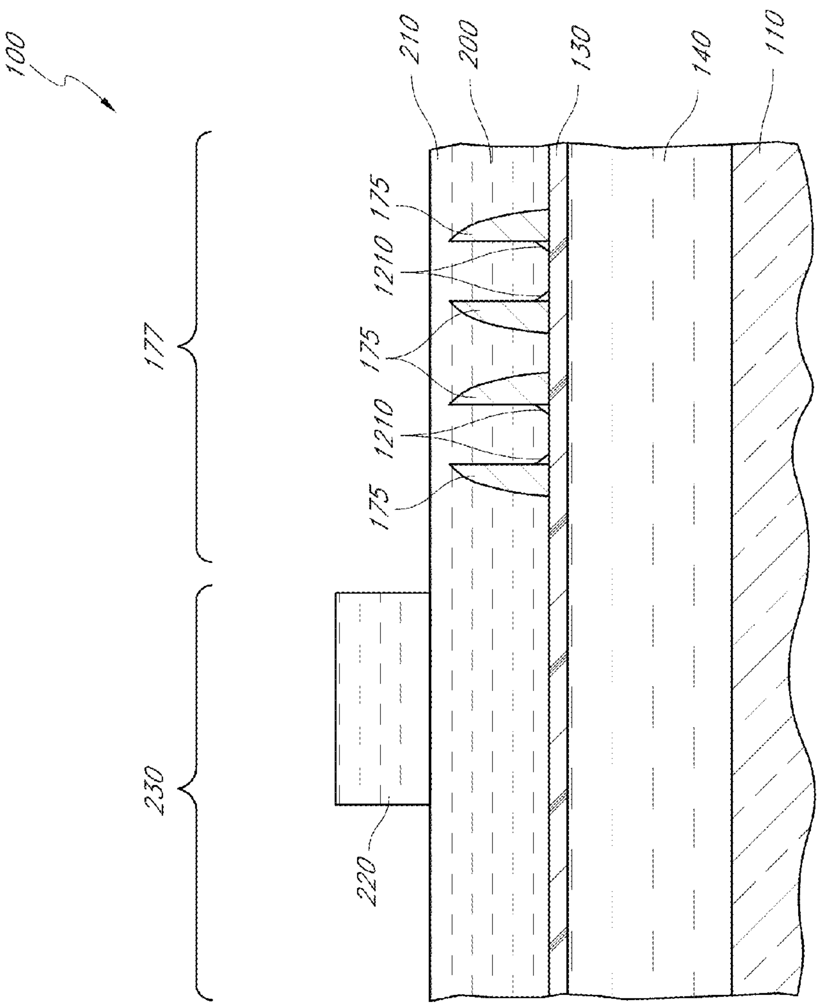


FIG. 13B

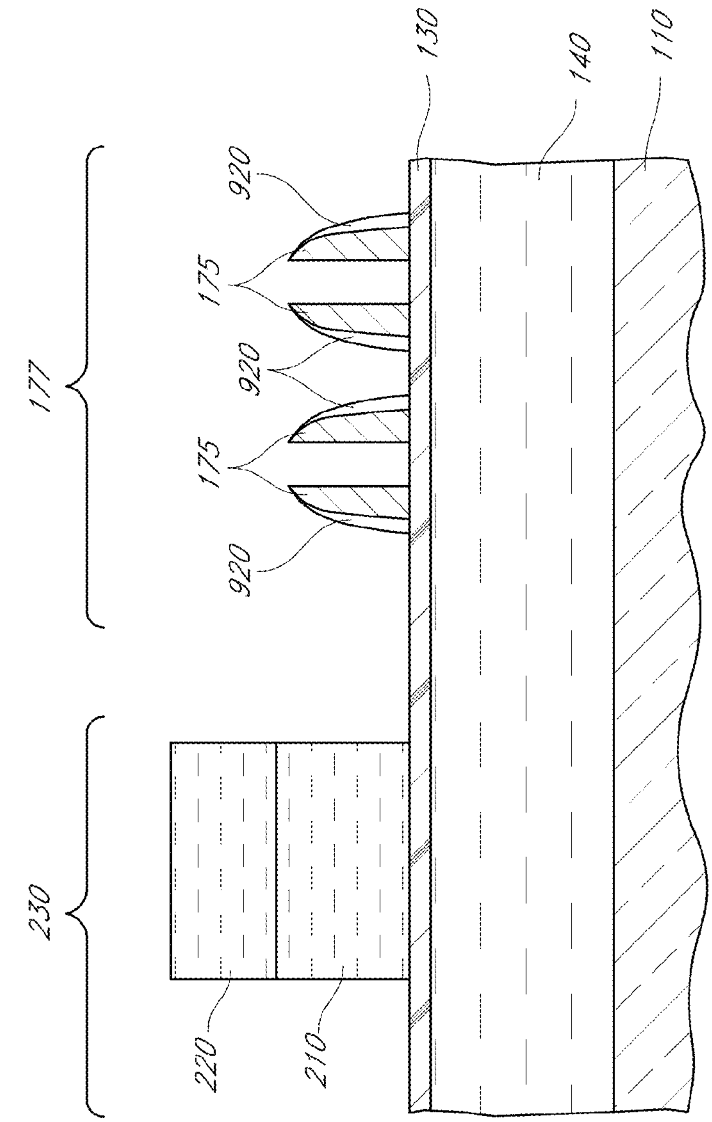


FIG. 14A

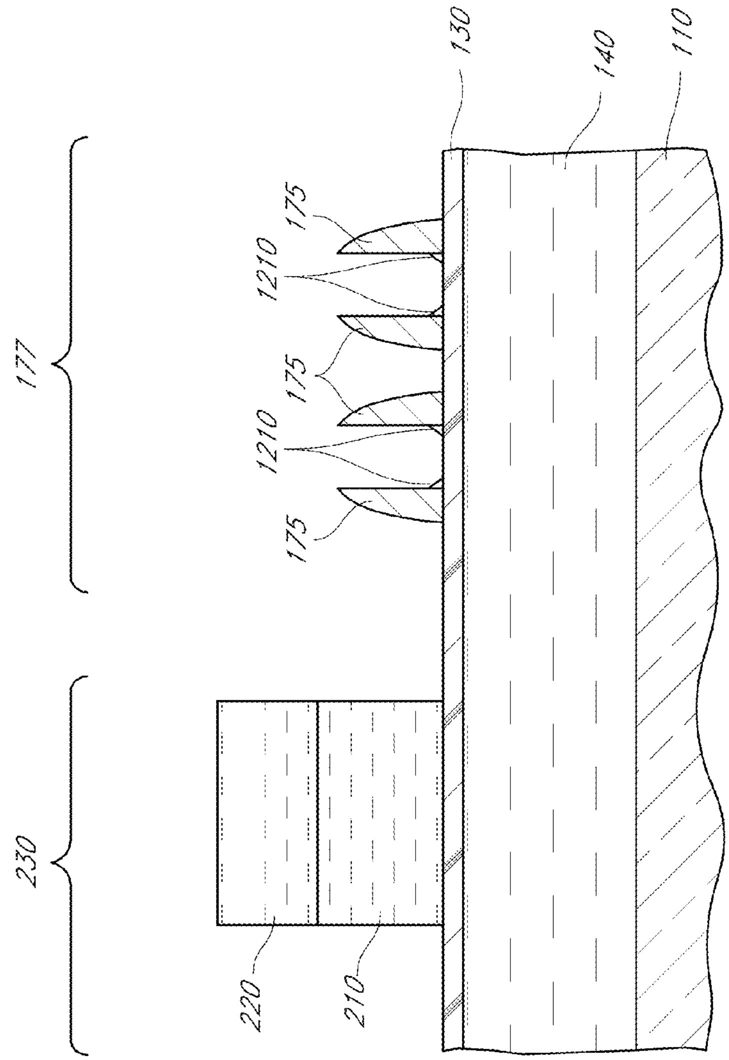


FIG. 14B

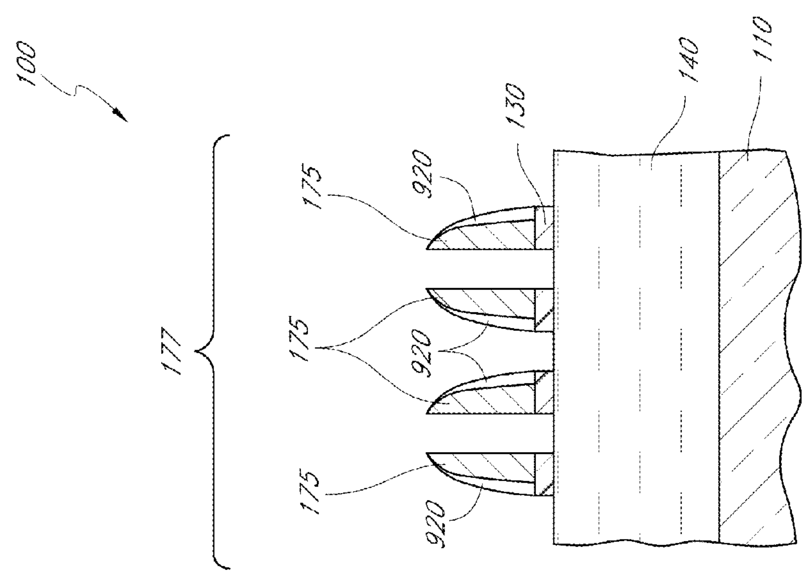


FIG. 15A

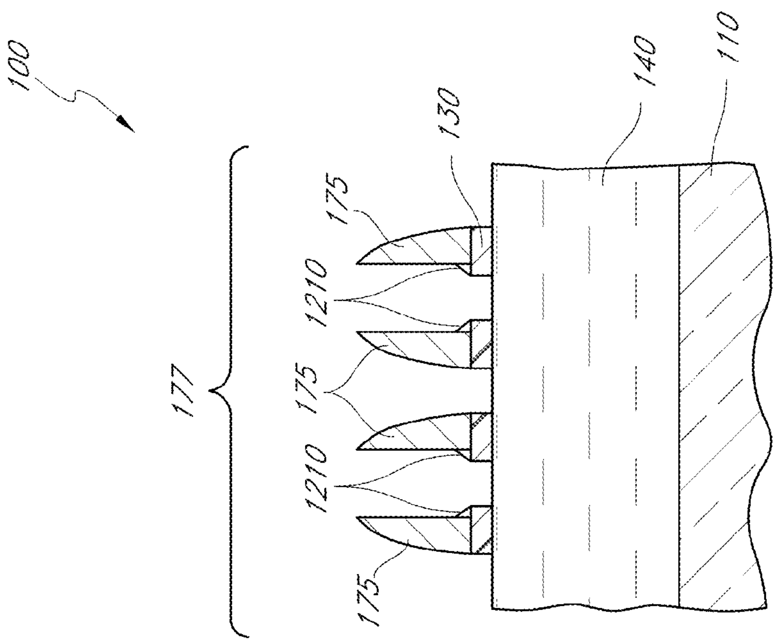


FIG. 15B

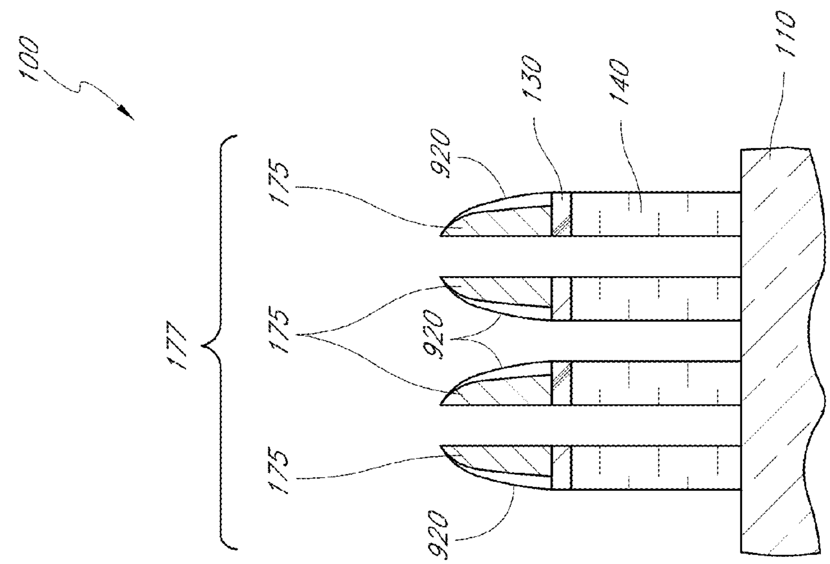


FIG. 16A

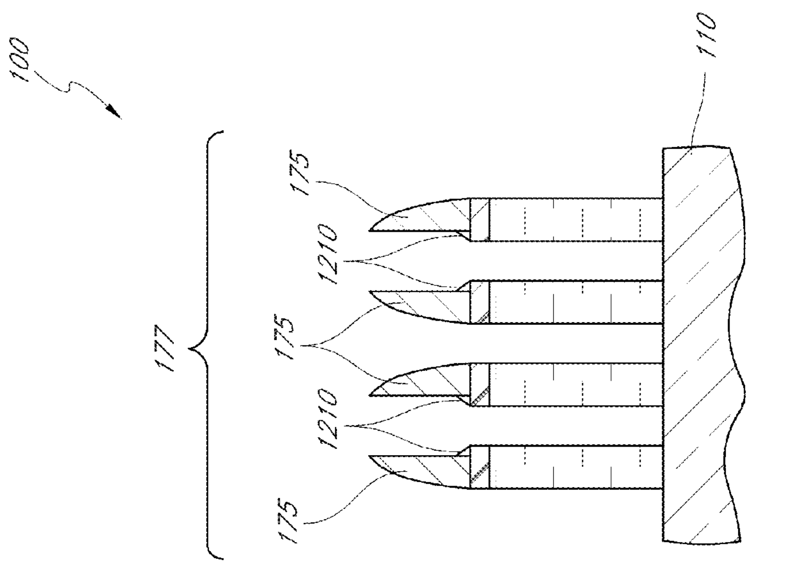


FIG. 16B

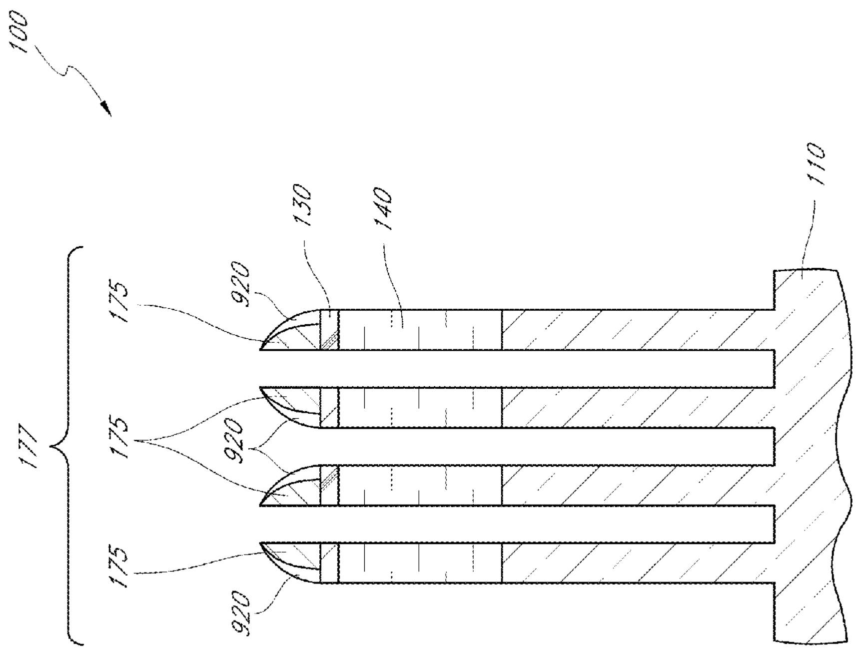


FIG. 17A

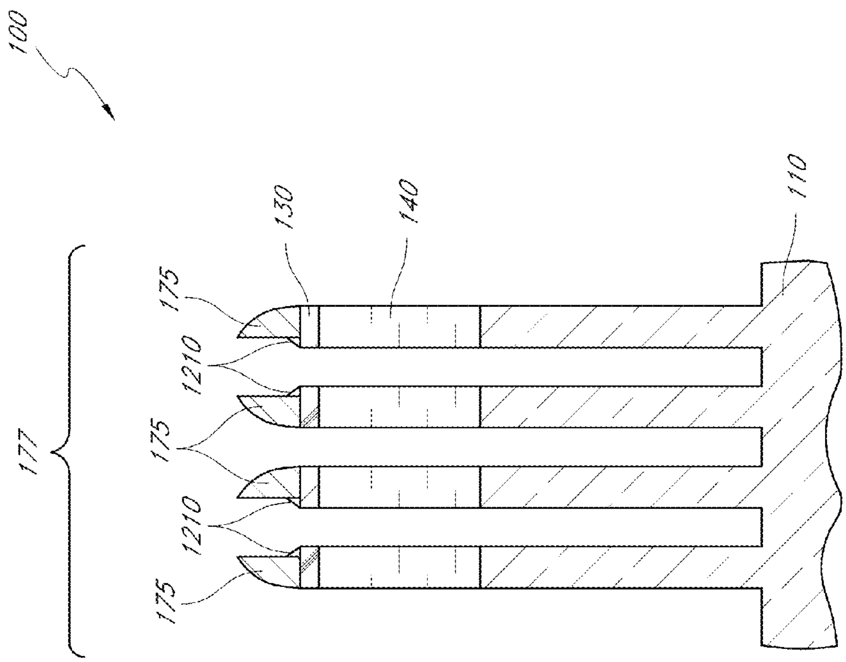


FIG. 17B

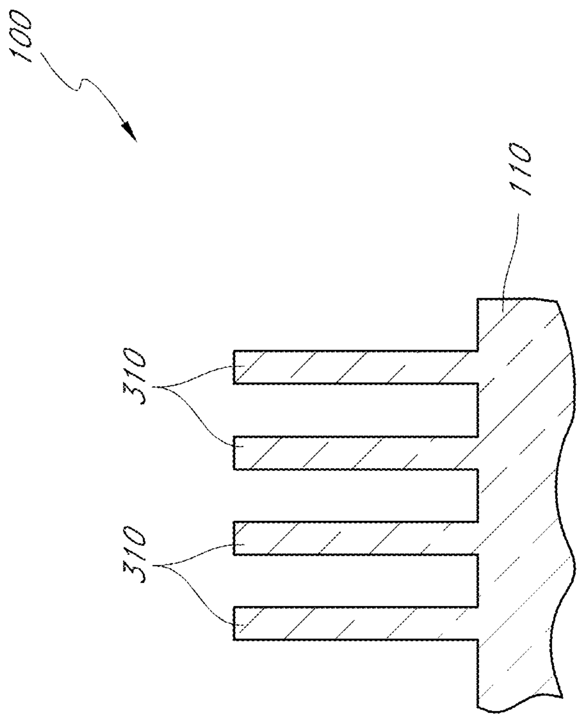


FIG. 18A

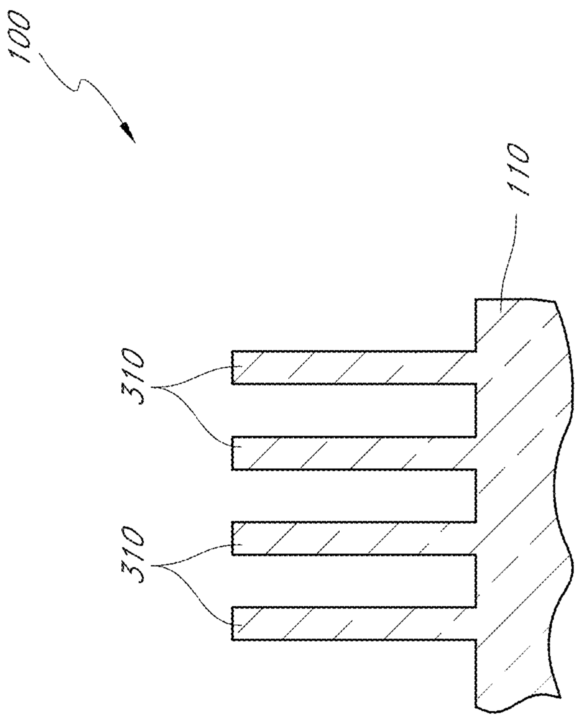


FIG. 18B

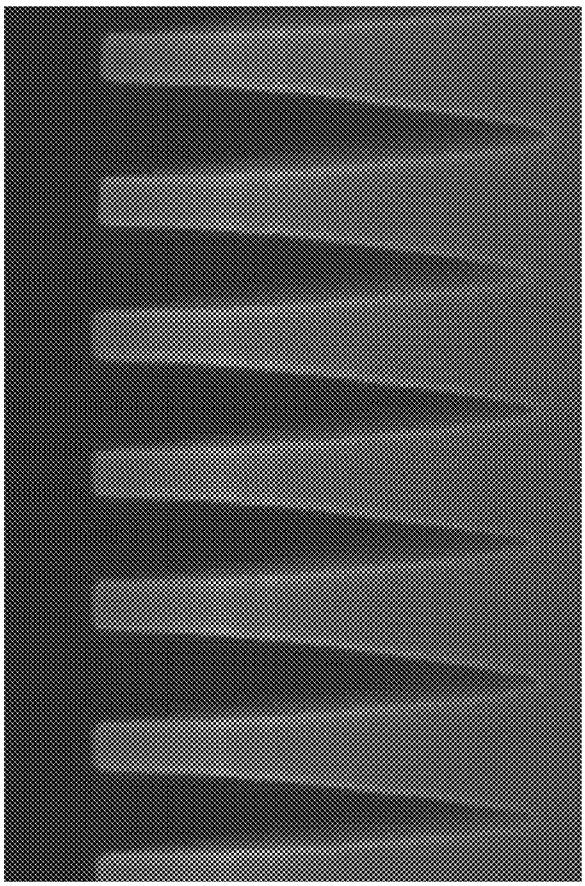


FIG. 19

METHOD FOR SELECTIVELY MODIFYING SPACING BETWEEN PITCH MULTIPLIED STRUCTURES

PRIORITY CLAIM

This application is a continuation of U.S. patent application Ser. No. 13/238,192, filed Sep. 21, 2011, entitled METHOD FOR SELECTIVELY MODIFYING SPACING BETWEEN PITCH MULTIPLIED STRUCTURES, which is a continuation of U.S. patent application Ser. No. 12/053,513, filed Mar. 21, 2008, entitled METHOD FOR SELECTIVELY MODIFYING SPACING BETWEEN PITCH MULTIPLIED STRUCTURES.

REFERENCE TO RELATED APPLICATIONS

This application is related to the following: U.S. patent application Ser. No. 10/934,778 to Abatchev et al., filed Sep. 2, 2004; U.S. patent application Ser. No. 11/214,544 to Tran et al., filed Aug. 29, 2005; and U.S. patent application Ser. No. 11/959,409 to Tran et al., filed Dec. 18, 2007.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the fabrication of integrated circuits and electronic devices and, more particularly, to fabrication methods and related structures.

2. Description of the Related Art

As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency, integrated circuits are constantly being reduced in size. The sizes of the constituent features that form the integrated circuits, e.g., electrical devices and interconnect lines, are also constantly being decreased to facilitate this size reduction.

The trend of decreasing feature size is evident, for example, in memory circuits or devices such as dynamic random access memories (DRAMs), flash memory, static random access memories (SRAMs), ferroelectric (FE) memories, etc. To take one example, DRAM typically includes millions or billions of identical circuit elements, known as memory cells. A memory cell typically consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that may store one bit (binary digit) of data. A bit may be written to a cell through the transistor and may be read by sensing charge in the capacitor.

In another example, flash memory typically includes billions of flash memory cells containing floating gate field effect transistors that can retain a charge. The presence or absence of a charge in the floating gate determines the logic state of the memory cell. A bit may be written to a cell by injecting charge to or removing charge from a cell. Flash memory cells may be connected in different architecture configurations, each with different schemes for reading bits. In a "NOR" architecture configuration, each memory cell is coupled to a bit line and may be read individually. In a "NAND" architecture configuration, memory cells are aligned in a "string" of cells, and an entire bit line is activated to access data in one of the string of cells.

In general, by decreasing the sizes of the electrical devices that constitute a memory cell and the sizes of the conducting lines that access the memory cells, the memory devices may be made smaller. Additionally, storage capacities may be increased by fitting more memory cells on a given area in the memory devices.

The concept of pitch may be used to describe one aspect of the sizes of features in an integrated circuit such as a memory device. Pitch is defined as the distance between identical points in two neighboring features, such as features in an array, which are typically arranged in a repeating pattern. These features are typically defined by spaces between adjacent features, which spaces are typically filled by a material, such as an insulator. As a result, pitch may be viewed as the sum of the width of a feature and of the width of the space on one side of the feature separating that feature from a neighboring feature. It will be appreciated that the spaces and features, such as lines, typically repeat to form a repetitive pattern of spacers and features.

Critical dimension (CD) is another term used to describe the sizes of features. The critical dimension is the smallest dimension of a feature in a particular circuit or masking scheme. Controlling the CD of certain structures, such as shallow trench isolation (STI) structures, during integrated circuit fabrication helps to facilitate the continued size reduction of integrated circuits by, e.g., ensuring predictable circuit performance.

The continual reduction in feature sizes places ever greater demands on the techniques used to form the features. For example, photolithography is commonly used to pattern features, such as conductive lines, in integrated circuit fabrication. However, due to factors such as optics, light or radiation wavelength and available photoresist materials, photolithography techniques may each have a minimum pitch or critical dimension below which a particular photolithographic technique cannot reliably form features. Thus, the inherent limitations of photolithographic techniques are obstacles to continued feature size reduction.

"Pitch doubling," which is also referred to as "pitch multiplication," is one proposed method for extending the capabilities of photolithographic techniques beyond their minimum pitch. A pitch multiplication method is illustrated in FIGS. **1**A-**1**F and described in U.S. Pat. No. 5,328,810, issued to Lowrey et al. With reference to FIG. **1**A, a pattern of lines **10** is photolithographically formed in a photoresist layer, which overlies a layer **20** of an expendable material, which in turn overlies a substrate **30**. As shown in FIG. **1**B, the pattern in the photoresist layer is transferred to the layer **20**, thereby forming placeholders, which are also referred to herein as mandrels, **40**. The photoresist lines **10** are stripped and the mandrels **40** are etched to increase the distance between neighboring mandrels **40**, as shown in FIG. **1**C. A layer **50** of spacer material is subsequently deposited over the mandrels **40**, as shown in FIG. **1**D. Spacers **60** are then formed on the sides of the mandrels **40**. The spacer formation can be accomplished by preferentially etching the spacer material from the horizontal surfaces **70** and **80**, as shown in FIG. **1**E. The remaining mandrels **40** are then removed, leaving behind only the spacers **60**, which together act as a mask for patterning, as shown in FIG. **1**F. Thus, where a given pitch previously included a pattern defining one feature and one space, the same width now includes two features and two spaces, with the spaces defined by the spacers **60**.

While the pitch is actually halved in the example above, this reduction in pitch is conventionally referred to as pitch "doubling," or, more generally, pitch "multiplication." Thus, conventionally, "multiplication" of pitch by a certain factor actually involves reducing the pitch by that factor. The conventional terminology is retained herein.

While allowing for smaller critical dimensions and pitch, pitch multiplication faces continuing development as new challenges emerge, as the requirements of integrated circuit fabrication change. Accordingly, there is a constant need for methods and structures for forming small features.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A-**1**F are schematic, cross-sectional side views of a sequence of masking patterns for forming conductive lines, in accordance with a prior art pitch multiplication method.

FIG. **2** is a schematic top plan view of a partially formed integrated circuit, in accordance with some embodiments of the invention.

FIGS. **3**A and **3**B are schematic cross-sectional side and top views of the partially formed integrated circuit of FIG. **2**, in accordance with some embodiments of the invention.

FIGS. **4**A and **4**B are schematic cross-sectional side and top plan views of the partially formed integrated circuit of FIGS. **3**A and **3**B after forming lines in a photoresist layer in an array region of the integrated circuit, in accordance with some embodiments of the invention.

FIGS. **5**A and **5**B are schematic cross-sectional side and top plan views of the partially formed integrated circuit of FIGS. **4**A and **4**B after widening spaces between lines in the photoresist layer, in accordance with some embodiments of the invention.

FIG. **6** is a schematic, cross-sectional side view of the partially formed integrated circuit of FIGS. **5**A and **5**B after depositing a layer of a spacer material, in accordance with some embodiments of the invention.

FIGS. **7**A and **7**B are schematic, cross-sectional side and top plan views of the partially formed integrated circuit of FIG. **6** after a spacer etch, in accordance with some embodiments of the invention.

FIGS. **8**A and **8**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **7**A and **7**B after removing a remaining portion of the temporary layer to leave a pattern of free-standing spacers, in accordance with some embodiments of the invention.

FIGS. **9**A and **9**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **8**A and **8**B after depositing augmentation material between and over the spacers, in accordance with some embodiments of the invention.

FIG. **10** is a scanning electron micrograph showing the spacers formed after a spacer etch, according to some embodiments of the invention.

FIG. **11** is a scanning electron micrograph showing the spacers after augmentation material deposition and the formation of an augmentation material bridge between spacers, according to some embodiments of the invention.

FIGS. **12**A and **12**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **9**A and **9**B after etching the augmentation material, in accordance with some embodiments of the invention.

FIGS. **13**A and **13**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **12**A and **12**B after forming another mask pattern overlying the substrate and before transferring the spacer pattern to the substrate, in accordance with some embodiments of the invention.

FIGS. **14**A and **14**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **13**A and **13**B where the mask pattern is transferred to a planarization layer on the same level as the spacer pattern in preparation for transfer to the underlying hard mask layer, in accordance with some embodiments of the invention.

FIGS. **15**A and **15**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **14**A and **14**B after forming a combined pattern defined by a patterned planarization material and the augmented spacers to an underlying hard mask layer, in accordance with some embodiments of the invention.

FIGS. **16**A and **16**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **15**A and **15**B after transferring the combined pattern to a primary mask layer, in accordance with some embodiments of the invention.

FIGS. **17**A and **17**B are schematic, cross-sectional side views of the partially formed integrated circuit of FIGS. **16**A and **16**B after transferring the combined pattern to the underlying substrate, in accordance with some embodiments of the invention.

FIGS. **18**A and **18**B are schematic, cross-sectional side and top views of the partially formed integrated circuit of FIGS. **17**A and **17**B after transferring the pattern into the substrate and removing hard mask layers overlying the substrate, in accordance with some embodiments of the invention.

FIG. **19** is a scanning electron micrograph showing features formed in a substrate, in accordance with some embodiments of the invention.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

A challenge in current pitch multiplication structures is achieving a desired balance between the inner and outer spaces. The inner and outer spaces are typically formed through a process of forming spaced apart mandrels, depositing a spacer material layer on the mandrels, directionally etching the spacer material layer, and removing the mandrels. This process results in spacers with substantially straight inner space walls, which were alongside the mandrels, and curved outer space walls on the side of the spacers without mandrels. As used herein, inner and outer space walls, which can also be referred to as sidewalls, can refer to opposite sides of the same spacer. Facing adjacent straight inner walls define the inner space and facing adjacent curved outer walls define the outer space. The spacers are used as a mask to etch underlying materials, such as hard masks and substrates. As a result, the spacing between spacers determines the spacing between later-formed features in the hard masks and substrates. Variations in process conditions and chemistries can cause the inner and outer spaces to be unbalanced, such that one is larger than the other. It will be appreciated that improving the uniformity between the inner and outer space is beneficial for improving the alignment of features formed using the spacers and for improving the reliability of the final product formed by the process. It has been believed that once the spacing between the free-standing spacers has been formed by the spacer formation process, the spacing cannot be selectively altered since the sides of the spacers are equally exposed to process gases.

Advantageously, some embodiments of the invention allow the inner or outer spaces to be selectively changed by laterally expanding the inner or outer sidewalls of spacers. Certain embodiments of the invention employ material deposition and/or etches that are selective with regard to the inner and outer spaces or walls.

In pitch multiplication, spacers typically have a straight inner wall and a curved outer wall due to formation of the spacers by etching a layer of spacer material. The curved outer wall is formed by greater exposure of the outer wall to etchant than the inner wall, which is typically adjacent to a mandrel that protects the inner wall from the etchant to a degree. Deposition and etching of an augmentation material on the spacers can be used to selectively grow or reduce the inner or outer space. Deposited material at the tops of the neighboring spacers tend to bridge together, e.g., seal, during the deposition such that the deposition in the inner space is blocked or slowed down but the deposition in the outer space is not similarly blocked or slowed down. As a result, the thickness of the deposited material is different between the inner to the outer spaces after the deposition and facilitates selective modifications of the widths of the inner and outer spaces. In some embodiments, the deposited material is a polymer, such as an organic polymer.

In certain embodiments where reduction of the outer space is desired, after deposition of the augmentation material, an etch at a high bias power is used. The etch is preferably an anisotropic etch at a bias power that is sufficiently high to remove the top bridge of material and the deposited augmentation material in the inner space. Since the inner space is not as heavily deposited as the outer space due to formation of the bridge between neighboring pairs of spacers limiting additional deposition, the inner space is etched more quickly during the etch. Therefore, the etch maintains the inner space substantially as it was before the deposition of augmentation material and helps to reduce the outer space since some deposited augmentation material still remains on the outer wall of the spacer, due to the higher levels of deposited material on the outer wall.

In certain embodiments where reduction of the inner space is desired, after deposition of the augmentation material, an etch at a relatively low bias power is used to etch the deposited augmentation material. The etch is preferably an anisotropic etch performed at a sufficiently low power to leave deposited material, which can also be referred to as footers, at corners in the inner space, the corners defined by the inner sidewall and an underlying material. While the invention is not limited by theory, because the inner sidewall is straight and the outer space is relatively widely open due to the curved outer sidewall, it is believed that this etching is more isotropic in the inner space but more anisotropic in the outer space. It is believe the relatively low bias power, in conjunction with the relatively narrow inner space, reduces the directionality of etchant species in the inner space while the relatively widely open outer space facilitates the directional movement of etchant species. The result of this differential etch behavior is that the outer sidewalls defining the outer space is relatively straight while the bottom of the inner space is rounded and has footers of deposited augmentation material on each sidewall. After the etch of the augmentation material, a pattern transfer etch of material underlying the spacers is applied. This pattern transfer etch has a high selectivity for the underlying material relative to the augmentation material. The rounded inner space bottom reduces the available opening for etching the underlying material, thereby narrowing the inner space for the pattern transfer. As a result, the pattern transferred to the underlying material has features corresponding to an inner space which is narrower than that formed initially after the spacer formation etch.

Reference will now be made to the Figures, wherein like numerals refer to like parts throughout. It will be appreciated that these Figures are not necessarily drawn to scale. Moreover, it will be appreciated that only a limited number of features, including mask features and etched features such as bit lines, word lines, spacers, and memory blocks are illustrated for ease of discussion and illustration. Different numbers of and/or positions for these features can be provided in some embodiments.

In a first phase of some embodiments of the invention, mask features are formed by pitch multiplication.

FIG. **2** shows a top view of a portion of a partially fabricated integrated circuit **100**. While the embodiments of the invention may be used to form any integrated circuit and may be applied to form masks for patterning various substrates, they may particularly advantageously be applied to form devices having arrays of electrical devices, including memory cell arrays for volatile and non-volatile memory devices such as DRAM, ROM or flash memory, including NAND or NOR flash memory, or integrated circuits having logic or gate arrays. For example, the logic array may be a field programmable gate array (FPGA) having a core array similar to a memory array and a periphery with supporting logics. Consequently, the integrated circuit **100** may be, e.g., a memory chip or a processor, which may include both a logic array and embedded memory, or any other integrated circuit having a logic or a gate array.

With continued reference to FIG. **2**, a central region **102**, which will be referred to hereinafter by example as the "array," is surrounded by a peripheral region **104**, which is often referred to hereinafter as the "periphery." It will be appreciated that, in a fully formed integrated circuit, such as a memory device, the array **102** will typically be densely populated with electrically conductive line and electrical devices, including transistors and/or capacitors. In a memory device, the electrical devices form a plurality of memory cells, which may be arranged in a regular grid pattern at the intersection of access lines and data lines, which are conventionally referred to in the industry as "word" lines and "bit" lines, respectively. Desirably, pitch multiplication may be used to form features such as rows/columns of transistors and/or capacitors in the array **102**, as discussed herein. On the other hand, the periphery **104** typically comprises features larger than those in the array **102**. Conventional photolithography, rather than pitch multiplication, is typically used to pattern features, such as logic circuitry, in the periphery **104**, because the geometric complexity of logic circuits located in the periphery **104** makes using pitch multiplication difficult, whereas the regular grid typical of array patterns is conducive to pitch multiplication. In addition, some devices in the periphery require larger geometries due to electrical constraints, thereby making pitch multiplication less advantageous than conventional photolithography for such devices. In some cases, the periphery **104** may contain patterns/circuits defined by both conventional lithography and pitch multiplication. In addition to possible differences in relative scale, it will be appreciated by the skilled artisan that the relative positions, and the number of periphery **104** and array **102** regions in the partially fabricated integrated circuit **100** may vary from that depicted.

FIG. **3**A shows a cross-sectional side view of the partially formed integrated circuit **100** and FIG. **3**B shows a top plan view of the integrated circuit **100**. With reference to FIG. **3**A various masking layers **120**-**140** are provided above a substrate **110**. The layers **120**-**140** will be etched to form a mask for patterning the substrate **110**, as discussed below. In the illustrated embodiment, a selectively definable layer **120** overlies a hard mask layer **130**, which can also be referred to as an etch stop, which overlies a primary mask layer **140**, which overlies the substrate **110** to be processed (e.g., etched) through a mask.

The materials for the layers **120**-**140** overlying the substrate **110** are chosen based upon consideration of the chemistry and process conditions for the various pattern forming and pattern transferring steps discussed herein. Because the layers between the topmost selectively definable layer **120** and the substrate **110** function to transfer a pattern derived from the selectively definable layer **120** to the substrate **110**, the layers **130**-**140** between the selectively definable layer **120** and the substrate **110** are chosen so that they may be selectively etched relative to other exposed materials. It will be appreciated that a material is considered selectively, or preferentially, etched when the etch rate for that material is at least about 2-3 times greater, at least about 10 times greater, at least about 20 times greater, or at least about 40 times greater than that for surrounding materials. Because a goal of the layers **120**-**130** overlying the primary hard mask layer **140** is to allow well-defined patterns to be formed in that layer **140**, it will be appreciated that one or more of the layers **120**-**130** may be omitted or substituted if suitable other materials, chemistries and/or process conditions are used. For example, where the substrate is relatively simple and may be selectively etched relative to the hard mask layer **130**, the primary mask layer **140** may be omitted and patterns may be transferred directly to the substrate using the hard mask layer **130**.

With continued reference to FIG. **3**A, the selectively definable layer **120** is photodefinable in some embodiments, e.g., formed of a photoresist, including any photoresist, including any positive or negative photoresist, known in the art. For example, the photoresist may be any photoresist compatible with 157 nm, 193 nm, 248 nm or 365 nm wavelength systems, 193 nm wavelength immersion systems, extreme ultraviolet systems (including 13.7 nm wavelength systems) or electron beam lithographic systems. In addition, maskless lithography, or maskless photolithography, may be used to define the selectively definable layer **120**. Examples of photoresist materials include argon fluoride (ArF) sensitive photoresist, i.e., photoresist suitable for use with an ArF light source, and krypton fluoride (KrF) sensitive photoresist, i.e., photoresist suitable for use with a KrF light source. ArF photoresists are used with photolithography systems utilizing relatively short wavelength light, e.g., 193 nm wavelength light. KrF photoresists are used with longer wavelength photolithography systems, such as 248 nm systems. In other embodiments, the layer **120** and any subsequent resist layers may be formed of a resist that may be patterned by nano-imprint lithography, e.g., by using a mold or mechanical force to pattern the resist.

In some embodiments, the material for the hard mask layer **130** comprises an inorganic material. Materials for the hard mask layer **130** include silicon oxide (SiO_2), silicon or an anti-reflective coating (ARC), such as a silicon-rich silicon oxynitride, a silicon-rich nitride, or a film that has the desired etch selectivity relative to the spacers **175** or other exposed materials (FIG. **7**A). In some embodiments, a Si, O, and N-containing spin-on hard mask with, for example, a 17% or a 43% Si content may be used for the layer **130**, which may be part of a multi-layer resist (MLR). The hard mask layer **130** may also include combinations of layers of materials, e.g., a bottom anti-reflective coating (BARC) over a dielectric anti-reflective coating (DARC). For ease of description, in the illustrated embodiment, the hard mask layer **130** is an anti-reflective coating, such as DARC. It will be appreciated that using ARCs for the hard mask layer **130** may be particularly advantageous for forming patterns having pitches near the resolution limits of a photolithographic technique. The ARCs can enhance resolution by minimizing light reflections, thus increasing the precision with which photolithography can define the edges of a pattern.

With continued reference to FIG. **3**A, embodiments of the invention may utilize the primary masking layer **140** to facilitate pattern transfer to a substrate. As noted above, in common methods of transferring patterns, both the mask and the underlying substrate are exposed to etchant, which may wear away a mask before the pattern transfer is complete. These difficulties are exacerbated where the substrate comprises multiple different materials to be etched. In some embodiments, the layer **140** is formed of a carbon-containing underlayer material.

In some other embodiments, due to its excellent etch selectivity relative to a variety of materials, including oxides, nitrides and silicon, the primary masking layer may be formed of amorphous carbon. The amorphous carbon layer may be formed by chemical vapor deposition using a hydrocarbon compound, or mixtures of such compounds, as carbon precursors. Carbon precursors may include propylene, propyne, propane, butane, butylene, butadiene and acetelyne. A method for forming amorphous carbon layers is described in U.S. Pat. No. 6,573,030 B1, issued to Fairbairn et al. on Jun. 3, 2003. In some embodiments, the amorphous carbon is a form of amorphous carbon that is highly transparent to light and that offers further improvements for photo alignment by being transparent to the wavelengths of light used for such alignment. Deposition techniques for forming such transparent carbon can be found in, e.g., A. Helmbold, D. Meissner, Thin Solid Films, 283 (1996) 196-203. In addition, the amorphous carbon may be doped as known in the art.

It will be appreciated that the "substrate" to which patterns are transferred may include a layer of a single material, a plurality of layers of different materials, a layer or layers having regions of different materials or structures in them, etc. These materials may include semiconductors, insulators, conductors, or combinations thereof.

With reference to FIGS. **4**A and **4**B, a pattern comprising spaces, such as trenches **122**, which are delimited by photodefinable material features **124**, is formed in the photodefinable layer **120**. The trenches **122** may be formed by, e.g., photolithography with 248 nm or 193 nm light, in which the layer **120** is exposed to radiation through a reticle and then developed. After being developed, the remaining photodefinable material, photoresist in the illustrated embodiment, forms mask features such as the illustrated lines **124** (shown in cross-section only).

The pitch of the resulting lines **124** is equal to the sum of the width of a line **124** and the width of a neighboring space **122**. To minimize the critical dimensions of features formed using this pattern of lines **124** and spaces **122**, the pitch may be at or near the limits of the photolithographic technique used to pattern the photodefinable layer **120**. For example, for photolithography utilizing 248 nm light, the pitch of the lines **124** may be about 100 nm. Thus, the pitch may be at the minimum pitch of the photolithographic technique and the spacer pattern discussed below may advantageously have a pitch below the minimum pitch of the photolithographic technique. Alternatively, because the margin of error for position and feature size typically increases as the limits of a photolithographic technique are approached, the lines **124** may be formed having larger feature sizes, e.g., 200 nm or more, to minimize errors in the position and sizes of the lines **124**.

As shown in FIGS. **5**A and **5**B, the spaces **122** are widened by etching the photoresist lines **124**, to form modified spaces **122*a*** and lines **124*a***. The photoresist lines **124** are etched using an isotropic etch to "shrink" or trim those features. Suitable etches include etches using an oxygen-containing plasma, e.g., a $SO_2/O_2/N_2/Ar$ plasma, a $Cl_2/O_2/He$ plasma or a $HBr/O_2/N_2$ plasma. The extent of the etch is selected so that the widths of the lines **124*a*** are substantially equal to the desired spacing between the later-formed spacers **175** (FIG.

7), as will be appreciated from the discussion below. For example, the width of the lines **124** may be reduced from about 80-120 nm to about 30-70 nm or about 50-70 nm. Advantageously, the width-reducing etch allows the lines **124***a* to be narrower than would otherwise be possible using the photolithographic technique used to pattern the photodefinable layer **120**. While the critical dimensions of the lines **124***a* may be etched below the resolution limits of the photolithographic technique, it will be appreciated that this etch does not alter the pitch of the spaces **122***a* and lines **124***a*, since the distance between identical points in these features remains the same.

Next, with reference to FIG. **6**, a layer **170** of spacer material is blanket deposited conformally over exposed surfaces, including the hard mask layer **130** and the top and sidewalls of the primary mask layer **140**. The spacer material may be any material that can act as a mask for transferring a pattern to the underlying hard mask layer **130**. The spacer material may be, without limitation, silicon, silicon oxide and silicon nitride. In the illustrated embodiment, the spacer material is silicon oxide, which provides particular advantages in combination with other selected materials of the masking stack.

Methods for spacer material deposition include atomic layer deposition, e.g., using a self-limiting deposition with a silicon precursor and a subsequent exposure to an oxygen or nitrogen precursor to form silicon oxides and nitrides, respectively. In some embodiments, to form silicon oxide, a silicon halide, such as silicon hexachlorodisilane (HCD), is introduced in alternating pulses with an oxygen precursor, such as H_2O. ALD can be performed at relatively low temperatures, e.g., under about 200° C. or under about 100° C., which has advantages for preventing thermal damage to underlying carbon-based materials, such as photoresist and amorphous carbon layers. In other embodiments, chemical vapor deposition is used to deposit the spacer material, e.g., using O_3 and TEOS to form silicon oxide.

The thickness of the layer **170** is determined based upon the desired width of the spacers **175** (FIG. 7A). For example, in some embodiments, the layer **170** is deposited to a thickness of about 20-80 nm or about 40-60 nm to form spacers of roughly similar widths. The step coverage is about 80% or greater and or about 90% or greater.

With reference to FIGS. **7**A and **7**B, the silicon oxide spacer layer **170** is subjected to an anisotropic etch to remove spacer material from horizontal surfaces **180** of the partially formed integrated circuit **100**.

With reference to FIGS. **8**A and **8**B, the selectively definable layer **120** is next removed to leave freestanding spacers **175**. The selectively definable layer **120** may be selectively removed using an organic strip process or various other etching processes.

Thus, pitch—multiplied mask features, the spacers **175**, have been formed. In the illustrated embodiment, the spacers **175** form elongated loops and have substantially parallel legs which are joined at their ends. The pitch of the spacers **175** is roughly half that of the photoresist lines **124** and spaces **122** (FIGS. **4**A and **4**B) originally formed by photolithography, but the pitch can vary due to process deviations, as discussed herein. For example, where the photoresist lines **124** had a pitch of about 200 nm, spacers **175** having a pitch of about 100 nm or less may be formed. It will be appreciated that because the spacers **175** are formed on the sidewalls of the features, such as lines **124***b*, the spacers **175** generally follow the outline of the pattern of lines **124***a* in the modified photodefinable layer **120***a* and, so, form a closed loop in the spaces **122***a* between the lines **124***a*.

Next, in a second phase of methods according to some embodiments of the invention, augmentation material is deposited on the spacers **175** and the augmentation material is etched to achieve a desired inner and outer space balance.

With continued reference to FIGS. **8**A and **8**B, the freestanding spacers **175** have straight inner walls **810** and curved outer walls **820**. The space between adjacent straight inner walls **810** defines the inner spaces **830**. The space between adjacent outer walls **820** defines the outer space **840**. Unless modified, imbalances between the widths of the inner space **830** and the outer space **840** will typically result in the formation of features having non-uniform transfer of the spacer pattern to the underlying substrate.

Process variations can cause the various imbalances between the widths of the inner space **830** and the outer space **840**. In certain embodiments, as shown in FIG. **8**A, the outer spaces **840** are larger in dimension than the inner spaces **830**. In other embodiments, as illustrated in FIG. **8**B, the inner spaces **830** are larger in dimension with respect to the outer spaces **840**.

Non-uniformities between the inner spaces **830** and the outer spaces **840** can be measured by methods known in the art. For example, in the case of a partially formed integrated circuit, a metrology tool can determine the positions of the spacers **175** and the relative dimensions of the inner and outer spaces **830**, **840**. The imbalance with respect to the spacers **175** can then be adjusted using methods herein described.

With reference to FIGS. **9**A and **9**B, augmentation material, e.g., polymer, is deposited, e.g., by chemical vapor deposition, between and over the spacers **175**. The deposition can be achieved in an etch chamber in which process conditions are selected to cause deposition of material on the spacers **175**. For example, in some embodiments, carbon-containing process gases such as CF_4 and CH_2F_2 are flowed into a reaction chamber having a RF power from about 300 W to about 1000 W and a RF bias voltage from about 150 V to about 500 V, with the ratio of CF_4:CH_2F_2 less than about 2.

Since the spacers **175** are formed having a straight inner wall **810**, which is straight relative to the curved outer wall **820**, the augmentation material is deposited more thickly over the curved outer wall **820** due to its increased surface area. As used herein, "inner wall" and "outer wall" can refer to opposite sides of the same spacer **175**. While the invention is not limited by theory, it is believed that the preferential deposition on the curved outer wall, in conjunction with the abrupt drop-off of the relatively straight inner wall **810**, cause the augmented material to begin bridging neighboring spacers **175** that have inner walls **810** facing each other. The inner wall **810** receives less deposited material due to its structural shape, but also because in some embodiments a bridge **910** may completely or partially form to block off any further deposition in between the inner walls **810**.

FIG. **10** shows a scanning electron micrograph of spacers formed after a spacer etch. FIG. **11** shows the spacers after augmentation material deposition and the formation of an augmentation material bridge between spacers.

With reference again to FIG. **9**A, augmentation material **920** is deposited onto the spacers **175** of FIG. **8**A, in which the outer spaces **840** are enlarged with respect to the inner spaces **830**. The augmentation material **920** deposition occurs preferentially on the curved outer wall **820**. In certain embodiments, however, as the deposition progresses, the deposited material begins to bridge the inner space **830**. The inner space **830** can become blocked by a bridge **910** forming between adjacent straight inner walls **810**. This prevents the addition of further augmentation material **920**, resulting in the growth of the outer wall **820** and reduction in the outer space **840**.

FIG. **9**B illustrates the deposition of augmentation material **920** onto the spacers **175** of FIG. **8**B, in which the inner spaces **830** are enlarged with respect to the outer spaces **840**. The augmentation material **920** deposition also occurs preferentially on the curved outer wall **820**, but in certain embodiments, due to the enlarged dimension of the inner space **830** relative to the outer space **840**, a greater degree of augmentation material **920** deposition occurs on the inner walls **810** of the spacers **175** than if the outer space **840** were larger than the inner space **830** (FIG. **9**A).

With reference to FIG. **12**A, a high bias voltage anisotropic etch is applied to etch the deposited polymer material. In one or more embodiments, the etch has a low oxygen content, which has advantages for controllably combusting and removing carbon species without completely removing deposited polymer material. This etch provides a substantially vertical inner wall **810**, and has a sufficiently high aggressiveness to substantially remove the deposited material on the inner wall **810**, but preserve a desired amount of deposited polymer on outer wall **820** to result in a desired net decrease in the width of the outer space **840** due to increasing the width of the spacers **175** on the outer wall **820** side of the spacers **175**. In certain embodiments, the anisotropic etch may include oxygen and a halide-containing etchant, the halides chosen from the group F, Cl, Br, and I. An example of a suitable etch chemistry includes HBr, O_2, and He. It will be appreciated that suitable etch conditions, including RF conditions, will vary depending on various factors, including the etching system, chemistries, deposited materials, and etch conditions used. In some embodiments, N_2 and/or Ar can be added to help stabilize the system. In some embodiments, the RF power is in the range from about 200 W to about 1000 W and the RF bias voltage is in the range from about 300 V to about 800 V.

FIG. **12**B illustrates a low bias voltage anisotropic etch (e.g., a plasma etch, which is often referred to as a "dry etch") performed on the structure of FIG. **8**B where the inner space **830** was larger relative to the outer space **840**. This etch has a sufficiently low aggressiveness to remove the augmentation material more gradually in the corners of the inner space **830** and more aggressively at the midpoints of the inner space or the outer spacer, such that footers **1210** remain on each side of the inner wall **810**. These footers **1210** function to increase the base width of the inner wall **810**, which decreases the effective width of the inner space **830** and narrows the exposed surface of the hard mask layer **130**.

The footers **1210** limit the etch of the underlying hard mask **130**, which thereby controls the transfer of the pattern from the combined augmentation material **920** and spacers **175** to the underlying hard mask layer **130**. In certain embodiments, the etch may include oxygen and a halide species. A suitable etch chemistry includes O_2, He, and CHF_3. As noted above, suitable etch conditions, including bias voltages, will vary depending on the etching system, chemistries, deposited materials, and etch conditions used. In some embodiments, the RF power is in the range from about 200 W to about 1000 W and the RF bias voltage is in the range from about 0 V to about 300 V.

Advantageously, the resulting spacers **175** have a desired spacing, which can be exceptionally uniform or non-uniform to a desired degree in some embodiments. In some embodiments, the spacers **175** can be used for defining a pattern in the substrate **110**, directly, without any intervening masking levels. In other embodiments, the pattern formed by the spacers **175** can be transferred to one or more masking levels before being transferred to the substrate **110**.

In some other embodiments as seen in FIGS. **13**A and **13**B, the spacers **175** are combined with another mask pattern before being transferred to the substrate **110**. For example, a planarization material **210** can be deposited around the spacers **175** and the planarization material **210** can be patterned to form a combined pattern with the spacers **175**. A selectively definable material **220** can be deposited over the planarization layer **210**. The selectively definable material **220** can then be patterned to form a second pattern **230** in a level above the spacers. For example, the selectively definable material **220** can be patterned by photolithography to define features in a periphery of the partially formed integrated circuit **100**. The second pattern is subsequently transferred to the planarization layer **210**, thereby being consolidated on the same level as the spacers **175**, as shown in FIGS. **14**A and **14**B. In other embodiments, the planarization material **210** can be a selectively definable material **220** such as photoresist, including positive or negative photoresist. The photoresist is then patterned to form the second pattern on the same level as the spacers **175**. The combined pattern formed by the patterned planarization layer and the spacers **175** can then be transferred to underlying layers or directly to the substrate **110**. In some other embodiments, a pattern is formed by etching an underlying hard mask layer using the spacers **175** as a mask and a planarization material is deposited about the features formed in the underlying hard mask layer, thereby allowing those features to be processed and combined with a second pattern as discussed above for the spacers **175**. Suitable methods for forming the second pattern in combination with spacers can be found in. e.g., U.S. patent application Ser. No. 11/214,544, filed Aug. 29, 2005.

With reference to FIGS. **15**A and **15**B, the spacer pattern **177** is transferred to the hard mask layer **130**. The pattern transfer may be accomplished by, e.g., anisotropically etching the hard mask layer **130**.

With reference to FIGS. **16**A and **16**B, the pattern **177** is transferred to the primary mask layer **140**. The pattern transfer may be accomplished by, e.g., anisotropically etching the primary mask layer **140**. With reference to FIGS. **17**A and **17**B, the pattern **177** is transferred to the substrate **110** using an anisotropic etch with the layer **140** acting as a mask for the etch.

With reference to FIGS. **18**A and **18**B, the spacers **175** and mask layers **130** and **140** overlying the substrate **110** are removed. Pitch multiplied lines **310** are formed in the substrate **110**. As seen in FIGS. **15**A-**18**B, the inner and outer space balancing of the spacers transfers to the hard mask layer **130**, the primary mask layer **140**, and the substrate **110**, such that the inner **830** and outer spaces **840** are substantially equalized. Advantageously, the resulting features have exceptionally uniform spacing as shown in the SEM of FIG. **19**.

Example 1

Silicon oxide spacers were augmented by deposition of a polymer in a reaction chamber of a 2300 Versys Kiyo from Lam Research Corporation of Fremont, Calif., United States. CF_4 and CH_2F_2 were flowed into the reaction chamber. The CF_4 was flowed at about 40 ccm and the CH_2F_2 was flowed at about 80 sccm. The substrate temperature was about 50° C. and the reaction chamber pressure was about 40 mTorr. The TCP power was about 500 W, the RF bias power was about 50 W and the RF bias voltage was about 265V.

The polymer deposition resulted in polymer bridging. The deposited polymer was etched to open the inner space. The etch chemistry included HBr, O_2, and He. The HBr was provided to the reaction chamber at a flow rate of about 90 sccm, the O_2 was flowed at about 60 sccm, and the He was flowed at about 120 sccm. The substrate temperature was about 50° C. and the reaction chamber pressure was about 5 mTorr. The TCP power was about 300 W, the RF bias power was about 0 W and the RF bias voltage was about 600V. Advantageously, the resulting spacers had a desirably narrowed outer space.

Example 2

Silicon oxide spacers were augmented by deposition and etching of a polymer in a reaction chamber of a 2300 Versys Kiyo from Lam Research Corporation of Fremont, Calif., United States. CF_4 and CH_2F_2 were flowed into the reaction chamber. The CF_4 was flowed at about 40 sccm and the CH_2F_2 was flowed at about 80 sccm. The substrate temperature was about 50° C. and the reaction chamber pressure was about 40 mTorr. The TCP power was about 500 W, the RF bias power was about 50 W, and the RF bias voltage was about 265V.

The polymer deposition resulted polymer bridging. The deposited polymer was etched to open the inner space. The etch chemistry included O_2, He, and CHF_3, provided to the reaction chamber. The O_2 was provided to the reaction chamber at a flow rate of about 60 sccm, the He was flowed at about 120 sccm, and the CHF_3 was flowed at about 90 sccm. The substrate temperature was about 50° C. and the reaction chamber pressure was about 15 mTorr. The TCP power was about 600 W, the RF bias power was about 0 W, and the RF bias voltage was about 150V. Advantageously, the resulting spacers had a desirably narrowed inner space.

It will be appreciated from the description herein that the invention includes various embodiments. For example, certain embodiments of the present invention provide a method for integrated circuit processing including providing a plurality of spacers overlying a material, depositing an augmentation material onto the plurality of spacers, the augmentation material bridging upper portions of pairs of neighboring spacers without bridging together upper portions of neighboring pairs of spacers, etching the augmentation material to form a pattern of augmented spacers, and transferring the pattern to the underlying material.

Certain other embodiments of the present invention provide a method of integrated circuit processing including selectively forming an augmentation material on an outer sidewall surface or an inner sidewall surface of a plurality of spacers, forming a pattern in an underlying material wherein features of the pattern are derived from the plurality of augmented spacers.

Certain embodiments of the present invention provide a method for patterning a substrate, including determining dimensions of an inner and outer space of a plurality of spacers, depositing a polymer onto the plurality of spacers, selecting an etch power to etch the polymer to achieve a desired open space dimension between the augmented spacers, and forming a pattern in an underlying substrate, wherein features of the pattern are derived from features of the augmented spacers.

Certain embodiments of the present invention provide a method for integrated circuit fabrication including providing a plurality of spacers, each spacer having an outer sidewall and an inner sidewall, the outer sidewall having a curved upper portion, wherein the inner sidewall is vertically straight relative to the outer sidewall. One of the inner or outer sidewalls of each spacer are substantially selectively laterally expanded.

It will also be appreciated by those skilled in the art that various omissions, additions and modifications may be made to the methods and structures described above without departing from the scope of the invention. All such modifications and changes are intended to fall within the scope of the invention, as defined by the appended claims.

What is claimed is:

1. A method for integrated circuit fabrication, comprising:
forming a memory array, wherein forming the memory array comprises:
forming a plurality of free-standing spacers over a substrate having an array region and a periphery region;
selectively forming an augmentation material on one side of each of the spacers to form a plurality of augmented spacers, the spacers and augmentation material extending across the array region; and
forming a pattern in the substrate, wherein features of the pattern are derived from the plurality of augmented spacers.

2. The method of claim 1, wherein selectively forming the augmentation material comprises preferentially depositing the augmentation material on the one side of each of the spacers.

3. The method of claim 2, wherein the spacers are formed by lines of spacer material alternating with open spaces, wherein preferentially depositing the augmentation material deposits augmentation material predominantly on sides of the spacers defining alternating ones of the open spaces, the alternating ones of the open spaces constituting a first set of open spaces.

4. The method of claim 3, wherein preferentially depositing the augmentation material forms bridges of augmentation material across tops of neighboring spacers defining a second set of open spaces alternating with open spaces of the first set, wherein the bridges block further deposition of augmentation material into the open spaces of the second set of open spaces.

5. The method of claim 4, wherein selectively forming the augmentation material comprises etching the bridge after depositing the augmentation material.

6. A method for integrated circuit fabrication, comprising:
providing a plurality of free-standing spacers over a substrate having an array region and a periphery region;
selectively forming an augmentation material on one side of each of the spacers to form a plurality of augmented spacers, the spacers and augmentation material extending across the array region; and
forming a first pattern in the substrate, wherein features of the first pattern are derived from the plurality of augmented spacers.

7. The method of claim 6, wherein providing the plurality of free-standing spacers comprises:
providing a plurality of mandrels;
blanket depositing a spacer material on the mandrels;
anisotropically etching the spacer material to define spacers on sidewalls of the mandrels; and
removing the mandrels to leave the free-standing spacers.

8. The method of claim 7, wherein providing the plurality of mandrels comprises performing photolithography, wherein the mandrels are formed of photoresist.

9. The method of claim 6, wherein selectively forming the augmentation material comprises depositing the augmentation material on the spacers and selectively removing the augmentation material from a side of each of the spacers.

10. The method of claim 9, wherein selectively forming the augmentation material forms a bridge of augmentation mate-

rial across some pairs of neighboring spacers, and wherein selectively removing the augmentation material comprises etching the bridge.

11. The method of claim **6**, wherein selectively forming the augmentation material comprises depositing a polymer.

12. The method of claim **11**, wherein depositing the polymer comprises chemical vapor depositing the polymer using a halogen-containing carbon precursor.

13. The method of claim **6**, wherein forming the first pattern in the substrate comprises selectively etching the substrate relative to the augmented spacers.

14. The method of claim **13**, wherein forming the first pattern in the substrate further comprises, before selectively etching the substrate:

depositing a protective layer over the augmented spacers;

patterning the protective layer to form a second pattern in the protective layer; and

simultaneously transferring the first and the second patterns to the substrate.

15. The method of claim **14**, wherein patterning the protective layer to form the second pattern comprises:

depositing a photoresist layer over the protective layer;

defining the second pattern in the photoresist layer; and

transferring the second pattern from the photoresist layer to the protective layer.

16. A method for integrated circuit fabrication, comprising:

providing a plurality of spaced-apart spacers over a substrate having an array region and a periphery region, each spacer having exposed first and second sidewalls on opposing sides of the spacer;

selectively laterally expanding one of the first or second sides of the spacers relative to the other of the first or second sides of the spacers, wherein the spacers are expanded across the array region; and

subsequently transferring a pattern defined by the spacers to an underlying material.

17. The method of claim **16**, wherein selectively laterally expanding comprises depositing mask material on the spacers.

18. The method of claim **17**, wherein selectively laterally expanding further comprises subjecting the deposited mask material to an etch to selectively remove the mask material from a side of each of the spacers.

19. The method of claim **18**, wherein subjecting the deposited mask material to the etch comprises performing the etch with a sufficiently low bias power to form footers of the mask material in spaces between pairs of neighboring spacers.

20. The method of claim **16**, wherein subsequently transferring the pattern comprises transferring the pattern to hard a mask layer overlying a substrate.

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